Fully Differential 3.6 GHz LC Voltage Controlled Oscillator

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***Abstract*—To design a fully-differential LC VCO, that meets or exceeds the given specifications using UMC 180nm technology.**

***Index Terms*—VCO, Phase Noise, Capacitance, Tuning, Divider, Buffer, Varactor**

I. Introduction

Voltage controlled Oscillator are tunable frequency sources which runs at very high frequency which are generally difficult to produce using crystal oscillators. Moreover any number VCOs can be integrated inside a chip as per requirement in contrast with crystal oscillators. It also allows flexibility in the implementation of tunable frequency sources as per the needs. They form very important part in PLL.

The desirable qualities of a VCO is high linearity, large tuning range, low phase noise, low power, appropriate output swing etc. The phase noise is very important parameter as it decides whether a VCO can be used for a particular modulation technique or not. That is why in this design instead of choosing directly $K_{vco} = 400MHz/V$, we are designing for $K_{vco} \simeq 50MHz/V$ with coarse and fine tuning technique.

II. Requirements

Sr. No	Property	Value
1.	Frequency	3.6 GHz
2.	Tuning Range	400 MHz
3.	Output Amplitude	1 V
4.	Phase Noise (1 MHz offset)	$\leq$ -117 dBc/Hz
5.	Phase Noise (20 MHz offset)	$\leq$ -145 dBc/Hz
6.	Supply Voltage	1.8V
7.	Power	Minimum
8.	Misc.	Divide-by-2
9.	Output phases @ 1.8 GHz	4
10.	K_{vco}	50 MHz/V

TABLE I: Requirements of the VCO

III. Topology

We have chosen mutually coupled inductor with NMOS negative-transconductance topology. This mutually coupled (symmetric) inductor provides higher Q than its single ended counterpart in IC implementation [3].

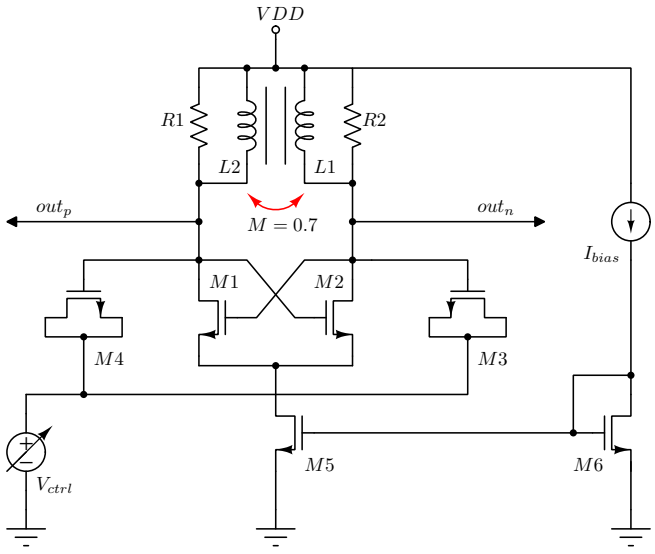

Fig. 1: Voltage controlled oscillator using symmetric inductor with MOS based Varactor

IV. Design

We started from Frequency 3.8 GHz as it the maximum frequency of interest and after adding capacitor bank the frequency will reduce for sure. Assuming nominal Q in chip to be 10 with operating frequency 3.8 GHz and L = 5nH, we calculate the required parallel R.

$$R = Q\omega_o L \tag{1}$$

$$\implies R \simeq 1.2\ K\Omega \tag{2}$$

So, required minimum g_m, (for startup condition)

$$g_m \geq \frac{1}{R} \tag{3}$$

$$\implies g_m \geq 0.84\ mA/V \tag{4}$$

The value of g_m would differ in actual implementation but this should act as starting point.

A. Capacitor banks

The capacitor bank should be made as symmetric as possible. It gives better result to make 2^n single capacitor-switch pair than a single capacitor-switch pair of value 2^nC as shown in Fig. 2. The turn-on resistance (R_{ds}) should be very low. The NMOS switch size may be 40um/180nm for optimal operation.

Minimum required number of coarse levels are

$$\frac{400\ MHz}{50\ MHz} = 8$$

. To guarantee that every frequency is achieved we require more number of levels. Here 4-bit (16-levels) capacitor bank is used to ensure that there are no blind-spots during frequency sweep.

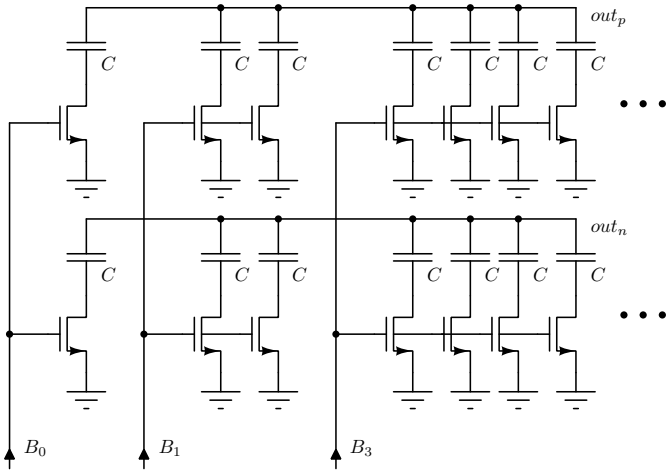

Fig. 2: 3-bit Capacitor Bank (only for illustration, actual circuit has 4-bit implementation); C = 50 fF

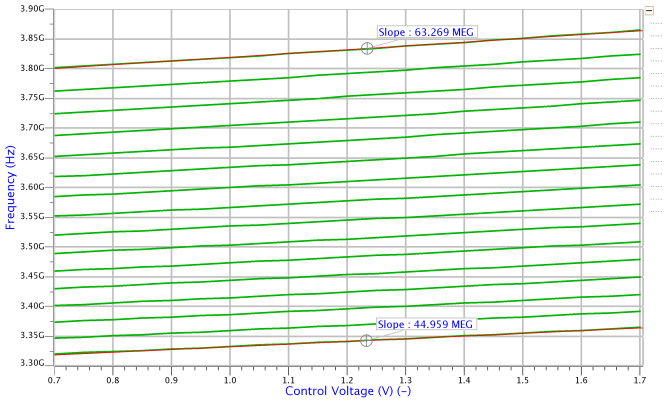

Fig. 3: Frequency vs. Control Voltage plots (showing 16 unique levels achieved using the capacitor bank); Average $K_{VCO} \simeq 50\ MHz/V$

B. Buffers

The buffers need to be designed carefully as the size of the devices can capacitively load the VCO core and change its frequency. However this can be solved by including the capacitance into the VCO core.

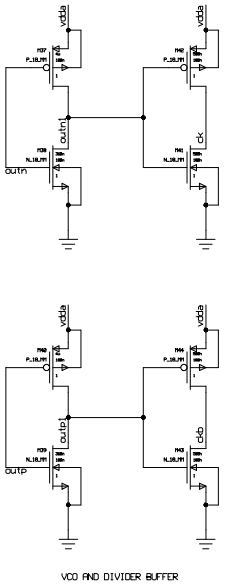

Fig. 4: Buffers (Between VCO and Divide-by-2 circuit)

As seen in Fig. 5 the common mode voltage is 1.8V so it requires large PMOS device to produce 50% duty cycle at the output. So, to alleviate this problem, the first inverter is designed so that it just barely convert the logic levels to 0-1.8 V. This is done so that minimum capacitance (which is highly non-linear) is added from the first inverter. Now to adjust the duty cycle properly to 50% it is now required to size the subsequent inverter by parameterised sweeping of PMOS/NMOS width.

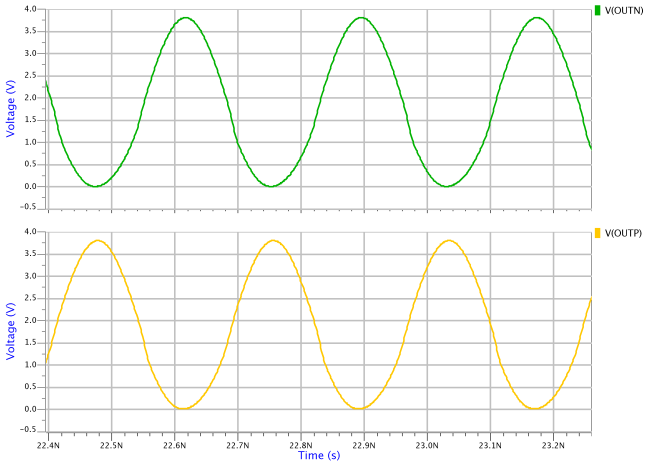

Fig. 5: Transient response of the VCO; Output amplitude achieved was 3.6 V

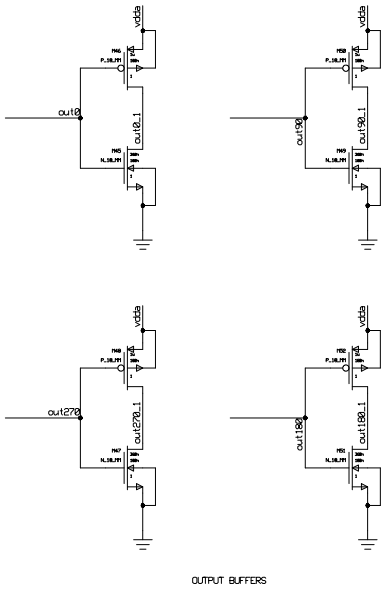

Fig. 6: Buffers (Between Divide-by-2 circuit and Output)

C. Varactor

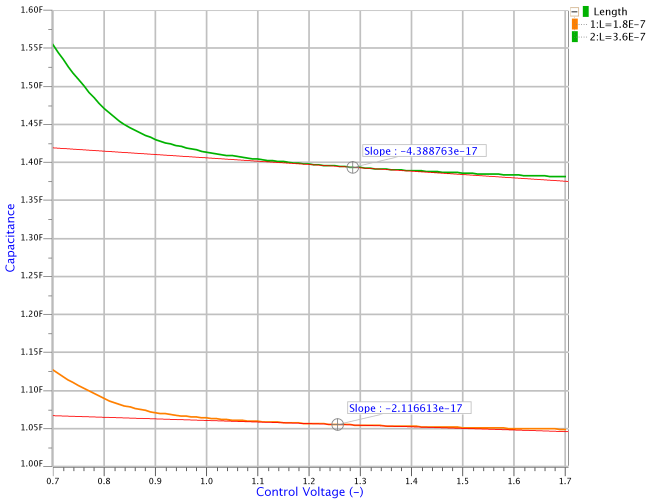

Fig. 7: Total capacitance ($C_{gs} + C_{gb} + C_{gd}$) of MOS device vs Control Voltage for a single 1um/180nm and 1um/360nm device.

Finding C_{min} for $f_{max} = 3.8\ GHz$ with L = 5nH

$$C_{min} = \frac{1}{L\omega_o^2} \tag{5}$$

$$\implies C_{min} = 351\ fF \tag{6}$$

We know,

$$f = \frac{1}{2\pi\sqrt{L(C_{min} + C_{var})}} \tag{7}$$

$$\frac{df}{dV} \simeq \frac{f}{2}\left(1 - \frac{C_{var}}{2C_{min}}\right)\frac{1}{C_{min}}\frac{dC_{var}}{dV} \tag{8}$$

$$\implies \frac{dC}{dV} = \frac{2K_{vco}C_{min}}{f\left(1 - C_{var}/2C_{min}\right)} \tag{9}$$

For first iteration assuming, $C_{var}/C_{min} \to 0$ and $K_{vco} = 50\ MHz/V$, $f = 3.8\ GHz$

$$\frac{dC}{dV} \simeq 9.237\ fF/V \tag{10}$$

Using Fig. 7, we choose L=360nm (to get twice the slope). Now we shall find the number of identical devices (N) required to achieve the required dC/dV.

$$N = \frac{9.237\ fF/V}{0.04389\ fF/V} \tag{11}$$

$$\implies N \simeq 210 \tag{12}$$

We can choose either 10 devices of 21um/360nm each or 210 devices 1um/360nm each. We must note that the slope is highly dependent on the configuration of devices chosen so, the later configuration would provide better closeness to calculations but it may be tedious handle 210 devices. Final N may vary depending on the other parameters during simulation.

D. Divider

At very high frequencies, special divider circuits have to used for 2 reasons :

1) Common T-flip-flop based Divide-by-2 circuits are too slow to generate proper voltage levels. The circuit inside them regularly violate setup time.
2) The phase noise deteriorate as the signal travels through more transistors. So, circuits having less number of transistors are usually preferred.

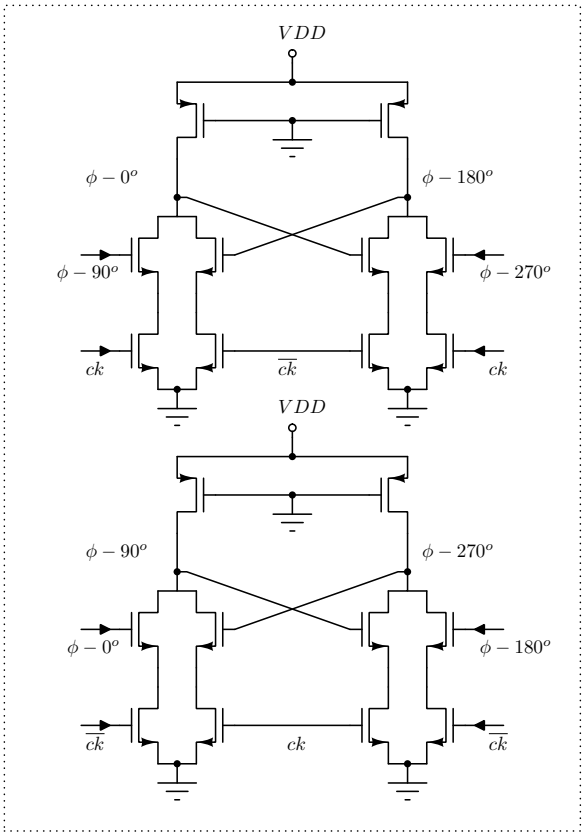

Fig. 8: Pseudo NMOS based Divide-by-2 circuit, also provides Quad phases [2] [1]

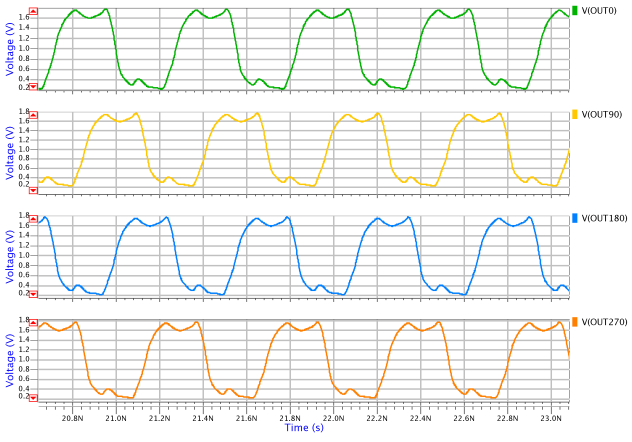

Fig. 9: Time domain response of the Divide-by-2 Circuit; Output amplitude achieved was 1.8 V (however not so clean) with almost 50% duty cycle

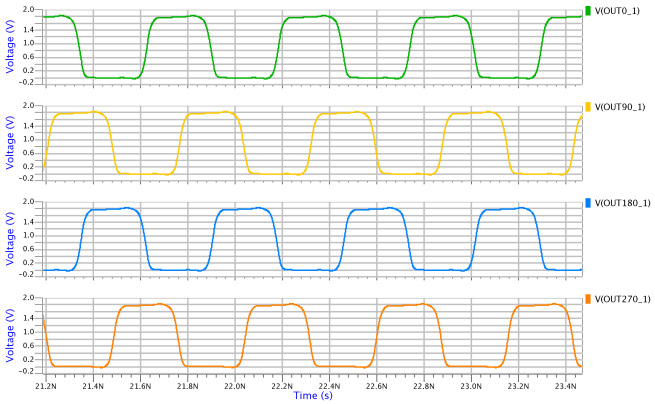

Fig. 10: Time domain response of Buffer placed after Divide-by-2 Circuit; Output amplitude achieved was 1.8 V with 50% duty cycle

V. Conclusions

All the requirements have been met with power consumption of 14.5 mW. The circuit is optimised for phase noise requirement as minimum number of transistors have been used.

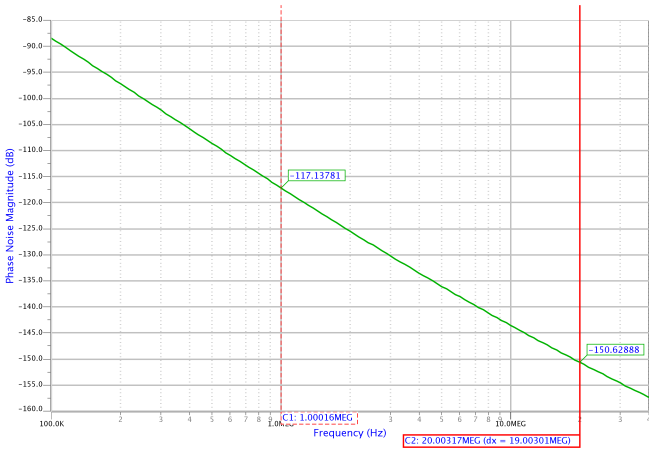

Fig. 11: Phase noise of the VCO operating at 3.6 GHz (V_{ctrl} = 1V and $V_0V_1V_2V_3 = 0110$); Phase noise = -117.138 dBc/Hz @ 1 MHz offset and -150.629 dBc/Hz @ 20 MHz

VI. Netlists

A. *Netlist.spi*

```
* ELDO netlist generated with ICnet by '
    ee18s063' on Fri Apr 26 2019 at
    07:16:31

.CONNECT GROUND 0

*
* Globals.
```

```
*
.global GROUND

*
* MAIN CELL: Component pathname : /home/
    ee18s063/Eldo_files/RFIC_EE6320/
    SS_VCO_REV0
*
M5 N$558 N$558 GROUND GROUND N_18_MM L
    =360n W=5u M=10
M42 CK OUTN1 VDDA VDDA P_18_MM L=180n W
    =500n M=1
C27 OUTP N$216 50f
C30 OUTP N$228 50f
C26 OUTP N$212 50f
M43 CKB OUTP1 GROUND GROUND N_18_MM L=180
    n W=500n M=1
R1 VDDA OUTN 1.9k NOISE=1
C24 OUTP N$204 50f
M31 N$208 B3 GROUND GROUND N_18_MM L=180n
     W=40u M=1
V4 B1 GROUND DC v1
C22 OUTP N$196 50f
V3 B0 GROUND DC v0
M10 N$124 B2 GROUND GROUND N_18_MM L=180n
     W=40u M=1
C3 OUTN N$120 50f
C25 OUTP N$208 50f
I1 VDDA N$558 DC 4m
M27 N$192 B2 GROUND GROUND N_18_MM L=180n
     W=40u M=1
C10 OUTP N$176 50f
V5 B2 GROUND DC v2
C19 OUTN N$168 50f
M26 N$188 B2 GROUND GROUND N_18_MM L=180n
     W=40u M=1
V6 B3 GROUND DC v3
C1 OUTN N$58 50f
C4 OUTN N$124 50f
M7 N$58 B0 GROUND GROUND N_18_MM L=180n W
    =40u M=1
C2 OUTN N$116 50f
M36 N$228 B3 GROUND GROUND N_18_MM L=180n
     W=40u M=1
C29 OUTP N$224 50f
M44 CKB OUTP1 VDDA VDDA P_18_MM L=180n W
    =500n M=1
M6 N$49 N$558 GROUND GROUND N_18_MM L=360
    n W=5u M=10
M22 N$156 B3 GROUND GROUND N_18_MM L=180n
     W=40u M=1
C15 OUTN N$152 50f
C28 OUTP N$220 50f
C20 OUTP N$188 50f
M40 OUTP1 OUTP VDDA VDDA P_18_MM L=180n W
    =4u M=1
M29 N$200 B3 GROUND GROUND N_18_MM L=180n
     W=40u M=1
M8 N$116 B1 GROUND GROUND N_18_MM L=180n
    W=40u M=1
C16 OUTN N$156 50f
M30 N$204 B3 GROUND GROUND N_18_MM L=180n
     W=40u M=1
C23 OUTP N$200 50f
M33 N$216 B3 GROUND GROUND N_18_MM L=180n
     W=40u M=1
C5 OUTN N$128 50f
M3 CTRL OUTP CTRL GROUND N_18_MM L=180n W
    =11u M=10
M64 N$578 CK GROUND GROUND N_18_MM L=180n
     W=500n M=1
M63 N$580 CKB GROUND GROUND N_18_MM L=180
    n W=500n M=1
M62 OUT0 OUT180 N$580 GROUND N_18_MM L
    =180n W=500n M=1
M61 OUT0 OUT90 N$578 GROUND N_18_MM L=180
    n W=500n M=1
V2 CTRL GROUND DC Vctrl
M12 N$132 B2 GROUND GROUND N_18_MM L=180n
     W=40u M=1
M13 N$136 B2 GROUND GROUND N_18_MM L=180n
     W=40u M=1
M23 N$160 B3 GROUND GROUND N_18_MM L=180n
     W=40u M=1
R2 VDDA OUTP 1.9k NOISE=1
M17 N$180 B1 GROUND GROUND N_18_MM L=180n
     W=40u M=1
M24 N$164 B3 GROUND GROUND N_18_MM L=180n
     W=40u M=1
C17 OUTN N$160 50f
M14 N$140 B3 GROUND GROUND N_18_MM L=180n
     W=40u M=1
C7 OUTN N$136 50f
M19 N$144 B3 GROUND GROUND N_18_MM L=180n
     W=40u M=1
M25 N$168 B3 GROUND GROUND N_18_MM L=180n
     W=40u M=1
C12 OUTP N$184 50f
M16 N$176 B1 GROUND GROUND N_18_MM L=180n
     W=40u M=1
C9 OUTP N$172 50f
M15 N$172 B0 GROUND GROUND N_18_MM L=180n
     W=40u M=1
M11 N$128 B2 GROUND GROUND N_18_MM L=180n
     W=40u M=1
M21 N$152 B3 GROUND GROUND N_18_MM L=180n
     W=40u M=1
M41 CK OUTN1 GROUND GROUND N_18_MM L=180n
     W=500n M=1
M4 CTRL OUTN CTRL GROUND N_18_MM L=180n W
    =11u M=10
C8 OUTN N$140 50f
```

```
M60 OUT0 GROUND VDDA VDDA P_18_MM L=180n
    W=320n M=1
M59 OUT180 GROUND VDDA VDDA P_18_MM L=180
    n W=320n M=1
M1 OUTN OUTP N$49 GROUND N_18_MM L=180n W
    =11u M=10
M2 OUTP OUTN N$49 GROUND N_18_MM L=180n W
    =11u M=10
M68 N$604 CKB GROUND GROUND N_18_MM L=180
    n W=500n M=1
M67 N$607 CK GROUND GROUND N_18_MM L=180n
     W=500n M=1
M66 OUT180 OUT270 N$607 GROUND N_18_MM L
    =180n W=500n M=1
M65 OUT180 OUT0 N$604 GROUND N_18_MM L
    =180n W=500n M=1
V1 VDDA GROUND DC 1.8
M9 N$120 B1 GROUND GROUND N_18_MM L=180n
    W=40u M=1
C6 OUTN N$132 50f
L1 vdda outp 5n
L2 vdda outn 5n
K1 L1 L2 0.7
M34 N$220 B3 GROUND GROUND N_18_MM L=180n
     W=40u M=1
C31 N$558 GROUND 500f
M32 N$212 B3 GROUND GROUND N_18_MM L=180n
     W=40u M=1
M38 OUTN1 OUTN GROUND GROUND N_18_MM L
    =180n W=360n M=1
M78 N$636 CK GROUND GROUND N_18_MM L=180n
     W=500n M=1
M77 N$639 CKB GROUND GROUND N_18_MM L=180
    n W=500n M=1
M76 OUT90 OUT180 N$639 GROUND N_18_MM L
    =180n W=500n M=1
M75 OUT90 OUT270 N$636 GROUND N_18_MM L
    =180n W=500n M=1
M20 N$148 B3 GROUND GROUND N_18_MM L=180n
     W=40u M=1
C13 OUTN N$144 50f
C18 OUTN N$164 50f
C14 OUTN N$148 50f
M35 N$224 B3 GROUND GROUND N_18_MM L=180n
     W=40u M=1
M18 N$184 B2 GROUND GROUND N_18_MM L=180n
     W=40u M=1
C11 OUTP N$180 50f
M52 OUT180_1 OUT180 VDDA VDDA P_18_MM L
    =180n W=wp M=1
M51 OUT180_1 OUT180 GROUND GROUND N_18_MM
     L=180n W=360n M=1
M50 OUT90_1 OUT90 VDDA VDDA P_18_MM L=180
    n W=wp M=1
M49 OUT90_1 OUT90 GROUND GROUND N_18_MM L
    =180n W=360n M=1
M48 OUT270_1 OUT270 VDDA VDDA P_18_MM L
    =180n W=wp M=1
M47 OUT270_1 OUT270 GROUND GROUND N_18_MM
     L=180n W=360n M=1
M46 OUT0_1 OUT0 VDDA VDDA P_18_MM L=180n
    W=wp M=1
M45 OUT0_1 OUT0 GROUND GROUND N_18_MM L
    =180n W=360n M=1
M74 N$626 CKB GROUND GROUND N_18_MM L=180
    n W=500n M=1
M73 N$628 CK GROUND GROUND N_18_MM L=180n
     W=500n M=1
M72 OUT270 OUT90 N$628 GROUND N_18_MM L
    =180n W=500n M=1
M71 OUT270 OUT0 N$626 GROUND N_18_MM L
    =180n W=500n M=1
M70 OUT270 GROUND VDDA VDDA P_18_MM L=180
    n W=320n M=1
M69 OUT90 GROUND VDDA VDDA P_18_MM L=180n
     W=320n M=1
M28 N$196 B2 GROUND GROUND N_18_MM L=180n
     W=40u M=1
C21 OUTP N$192 50f
M39 OUTP1 OUTP GROUND GROUND N_18_MM L
    =180n W=360n M=1
M37 OUTN1 OUTN VDDA VDDA P_18_MM L=180n W
    =4u M=1
*
.end
```

B. SS_VCO_REV0_default_default.cir

```
* Component: /home/ee18s063/Eldo_files/
    RFIC_EE6320/SS_VCO_REV0 Viewpoint:
    default

.OPTION COMPAT
.INCLUDE "/home/ee18s063/Eldo_files/
    RFIC_EE6320/SS_VCO_REV0/default/
    netlist.spi"
.OPTION AEX
.OPTION ENGNOT
.OPTION LIMPROBE=10000.0
.OPTION NOASCII
.ic v(outp)=2
.ic v(outn)=0.5
.EXTRACT DC LABEL = gm1 GM(M1)
.EXTRACT DC LABEL = gm2 GM(M2)
.EXTRACT DC LABEL = cgb3 CGB(M3)
.EXTRACT DC LABEL = cgd3 CGD(M3)
.EXTRACT DC LABEL = cgs3 CGD(M3)
.EXTRACT DC LABEL = cgb2 CGB(M2)
.EXTRACT DC LABEL = cgs2 CGS(M2)
.EXTRACT DC LABEL = cgd2 CGD(M2)
.EXTRACT DC LABEL = C cgb3+cgd3+cgs3+cgb2
   +cgd2+cgs2
.plot sstnoise db(sphi)
```

```
* -- Analysis Setup -- DCOP
.OPTION PROBEOP2
.OP

* -- Analysis Setup -- SST
.SST OSCIL FUND_OSC_GUESS1=3.6G
    NHARM_OSC1=30
+ VCONTROL=V2
.SSTPROBE OUTP OUTN FUND_OSC
.EXTRACT FSST LABEL=Osc_Freq FUND_OSC

* -- Analysis Setup -- SST Noise
.SSTNOISE V(OUTP, OUTN) HARM(1) DEC 50
    100k 40Meg XAXIS=FREQ_COMMAND
.PLOT SSTNOISE DB(INOISE)
.PLOT SSTNOISE DB(ONOISE)
.PLOT SSTNOISE DB(PHNOISE)
.PLOT SSTNOISE DB(AMNOISE)

* --- Global Outputs
.PROBE V SG

* --- Params
.TEMP 27.0
.PARAM v0=0
.PARAM v1=1.8
.PARAM v2=1.8
.PARAM v3=0
.PARAM Vctrl =1
.PARAM Ibias=4m

* --- Libsetup
.LIB KEY=TT "/home/ee18s063/Eldo_files/
    Models_UMC180/MM180_REG18_V124.lib" TT
```

REFERENCES

[1] High Speed Communication Circuits and Systems, Lecture-14, High Speed Frequency Dividers, Michael Perrott, Massachusetts Institute of Technology

[2] Krishnapura et. al, A 5.3 GHz Programmable Divider for HiPerLan in 0.25m CMOS, JSSC, July 2000

[3] Chapter 7 - Behzad Razavi. 2011. RF Microelectronics (2nd Edition) (Prentice Hall Communications Engineering and Emerging Technologies Series) (2nd ed.). Prentice Hall Press, Upper Saddle River, NJ, USA

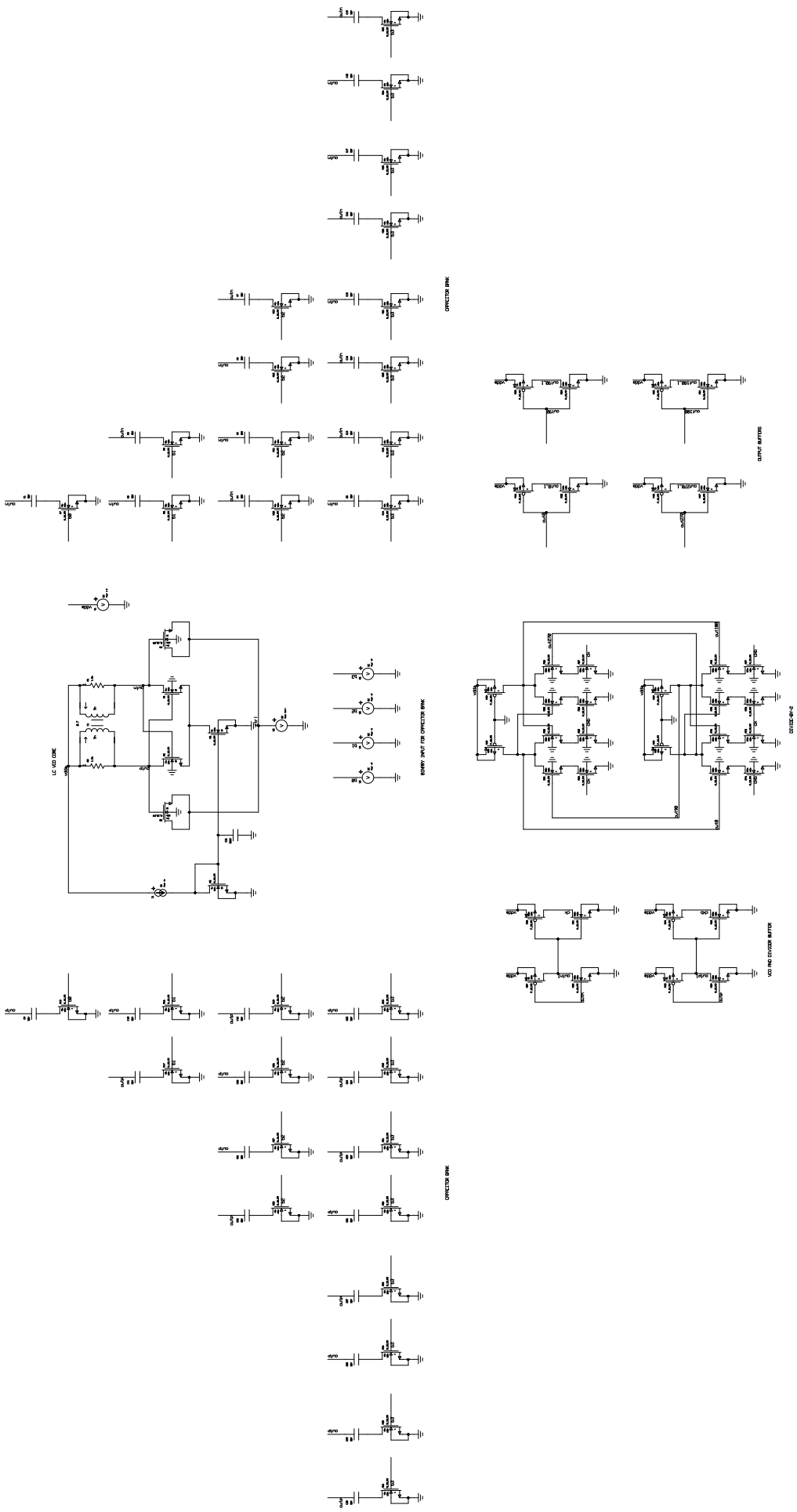

Fig. 12: Schematic of the entire VCO in Pyxis (Netlist is attached)