Fully Differential Double-Balanced Gilbert-Cell IQ Mixer

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***Abstract*—To design a fully-differential double-balanced Gilbert-cell IQ mixer to be used in a direct-conversion receiver, that meets or exceeds the given specifications using UMC 180nm process models that was used for the LNA project.**

***Index Terms*—Mixer, Noise Figure, S-parameters, IIP3, IIP2, SNR, Baluns, LNA, Conversion gain**

I. Introduction

The mixer in this project is used to downconvert the high frequency RF signals to Baseband signal. Mixer is time variant system because the Large signals at LO (and sometimes at RF port also) changes the system's operating point within one time period. The most reliable way to simulate such system is performing transient analysis and then finding FFT to find the frequency spectrum. But such transient analysis takes a lot of time and memory (because of presence of both very low frequency signal (message) and high frequency signal (carrier)). So, to simplify and speed up preliminary simulations, we use 2 methods to simulate such Linear Time Variant System.

1) By assuming RF port to be small signal (may be non-linear too) and LO to be large signal. Advantage is that the simulation is very fast compared to second method as PSS is done for LO port (one period waveform is extracted, and frequency spectra is calculated) while AC is done for RF port. The convolution of AC response with frequency spectra of PSS is the final result. We have to specify the harmonics to find the result. Apparently the response of one port due to another port is considered independent.
2) By assuming both RF port and LO port as Large signal and hence both are subjected to PSS analysis. Frequency spectra are calculated for the waveform found from each port and convolution is done. We finally do a sweep of RF frequency from $f_{LO} - f_{IF}$ to $f_{LO} + f_{IF}$ which increases the simulation time within acceptable limits.

We will follow the second process here, as the number of input ports are only 2 and carrier signal is not being modulated by any low frequency signal. However IF signal would be of low frequency which would be available using convolution of LO and RF spectra.

II. Requirements

Sr. No	Property	Value
1.	R_{in}	50Ω (single ended)
		100Ω (differential)
2.	R_{out}	50Ω (single ended)
		100Ω (differential)
3.	NF	$\leq 15dB$
4.	IIP_3	$\geq -11dBm$
5.	Supply Voltage	1.8V
6.	Power	Minimum
7.	S_{11}	$\leq -10dB$
8.	Conversion Gain	$\geq 15dB$
9.	Frequency	$1.8GHz$
10.	Band	$1.7GHz - 1.9GHz$

TABLE I: Requirements of the Mixer

III. Topology

We are using Source degenerated Common source stage as input transonductance stage to get better linearity (better IIP3). Unlike LNA, we cannot use same transformer (Inductor coupled) at the output (IF port). This is because the Inductor would offer low impedance at required IF frequency (20MHz) and hence low conversion gain.

Conversion gain is defined as the difference in power between the desired IF output power level (in dBm) and the input (RF) power level (in dBm). In simulation we can measure the voltage conversion gain only.

$$Gain = 10\log\frac{P_{out}}{P_{in}} = 10\log\frac{V_{out,rms}^2/4R_{out}}{V_{in,rms}^2/4R_{in}} \quad (1)$$

$$= 20\log\frac{V_{out,rms}}{V_{in,rms}} + 10\log\frac{R_{in}}{R_{out}} \quad (2)$$

From the above equations it is clear that if R_{out} is greater than R_{in} than the power conversion gain is smaller than the voltage conversion gain. If $R_{out} = R_{in}$ then Voltage gain equals power gain. Here R_{in} is defined as 50Ω. In Integrated IC level design, we worry more about the voltage conversion gain because the impedance (of next stage) is mostly capacitive which draws no real power. Also the conductor paths are too small to be considered enough for reflection. However

in discrete ICs, the output drives a 50Ω impedance line. For the sake of convenience in Gain measurement (and also assuming discrete IC mixer), we consider output impedance equals input impedance. This ambiguity in specification can lead to higher power consumption in this design because of less output impedance (resistance) which leads to larger MOS transistors and subsequently more current consumption.

IV. Design

To fit better with theory (which revolves around square law model), we choose larger length MOS devices ($\geq 0.5\mu m$). We start with $\omega_t L_s = 50\Omega$.

$$\omega_t = 38.37\ Grad/s \tag{3}$$
$$\implies L_s = 1.3\ nF \tag{4}$$

Resonant Frequency,

$$1.8GHz = \frac{1}{2\pi\sqrt{(L_s + L_g)C_{gs}}} \tag{5}$$

Using OP analysis,

$$C_{gs} = 2.64pF \tag{6}$$
$$\implies L_g = 1.65nF \tag{7}$$

We know output voltage (in RMS),

$$V_{out,IF} = \frac{2}{\pi} g_m R_D . V_{in,RF} \tag{8}$$

Where R_D = R_1 = R_4. When output is attached to balun (Fig. 3(c))

$$P_{out,IF} = \left(\frac{2}{\pi} g_m (R_{out} || R_D) . V_{in,RF}\right)^2 / R_D \tag{9}$$

Input power (During Match),

$$P_{in,RF} = \frac{V_{in,RF}^2}{4R_{in}} \tag{10}$$

Since R_{in} = R_D = R_{out}, from above we get

$$Gain(dB) = 20\log\left(\frac{2}{\pi} g_m R_D\right) \tag{11}$$

Equating the above equation with 15dB, we get (at perfect match)

$$g_m = 176.6mA/V \tag{12}$$

Practically the output $R_D \neq R_{out}$, for our case it is $R_D = 115\Omega$ & $R_{out} = 50\Omega$. Using 9,

$$g_m = 126.9mA/V \tag{13}$$

Using simulation g_m (transconductance inclusive of all multipliers), W/L, N (multiplier) is found to be,

$$g_m = 101.6mA/V \tag{14}$$
$$\frac{W}{L} = \frac{40\mu m}{540nm} \tag{15}$$
$$N = 20 \tag{16}$$

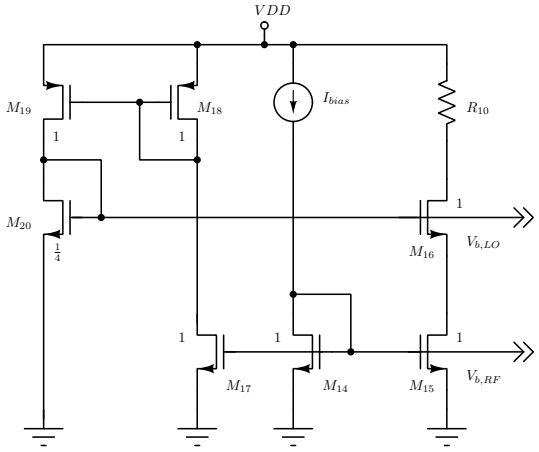

Fig. 1: Mixer Bias Circuit

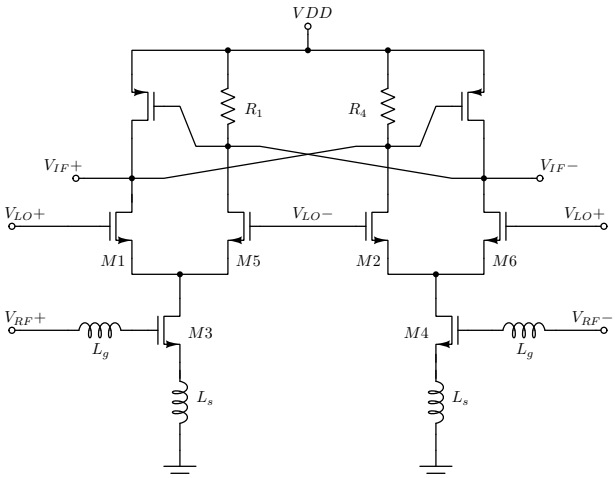

Fig. 2: Double Balanced Gilbert Cell Mixer

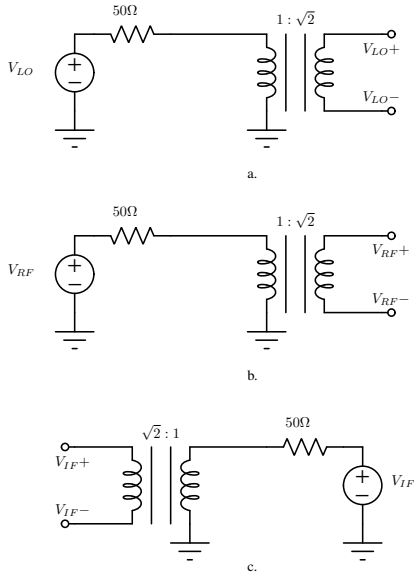

Fig. 3: Baluns

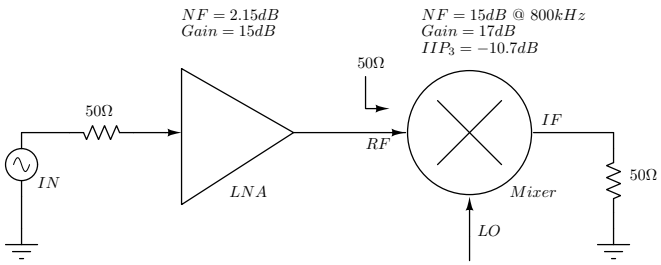

Fig. 4: Diagram of Mixer preceded by LNA

V. Results

Please refer Fig. 5, 6, 7, 8, 9 for mixer only. Refer Fig. 10, 11, 12, 13 for LNA-Mixer system.

Calculated,

$$IIP3 = -10.7dBm - 15dB = -25.7dBm$$

$$NF = 1 + (10^{2.15/10} - 1) + \frac{10^{15/10} - 1}{5.62^2}$$

$$= 4.39dB$$

$$Gain = 15dB + 17dB = 32dB$$

Sr. No	Property	Calculated	Simulated
1.	Conversion Gain	$32dB$	$33.75dB$
2.	NF	$4.39dB$	$4.25dB$
3.	IIP3	$-25.7dBm$	$-26.0dBm$

TABLE II: Comparision Table between hand calculated values and simulated values

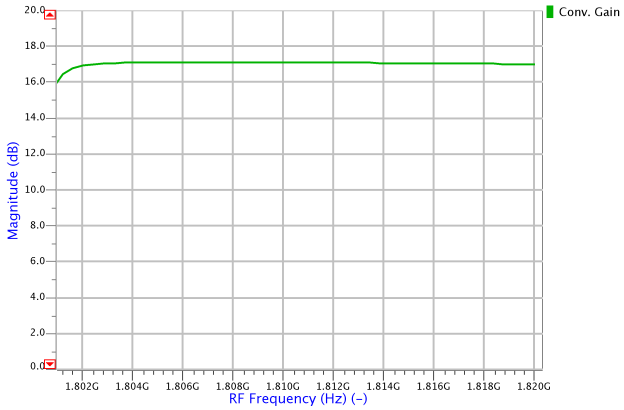

Fig. 5: Conversion gain of Mixer, Conversion Gain = 17dB

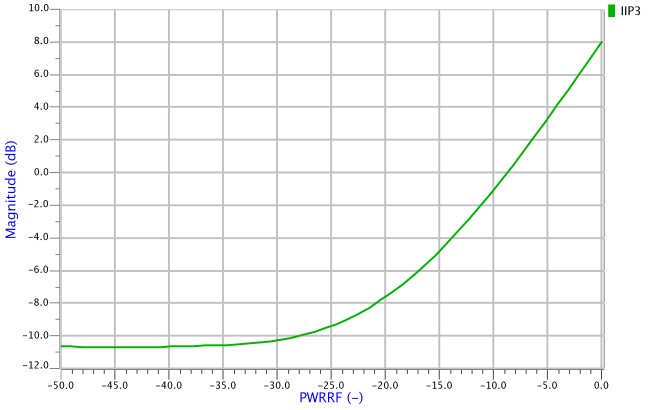

Fig. 6: Input 3^{rd} order Intermodulation Intercept Point (IIP3) of the Mixer (IF port), IIP3 = -10.7dBm

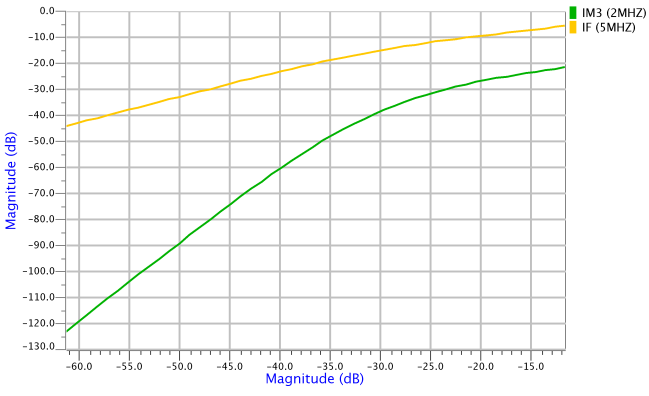

Fig. 7: Plot showing the Fundamental IF component along with intermodulation component

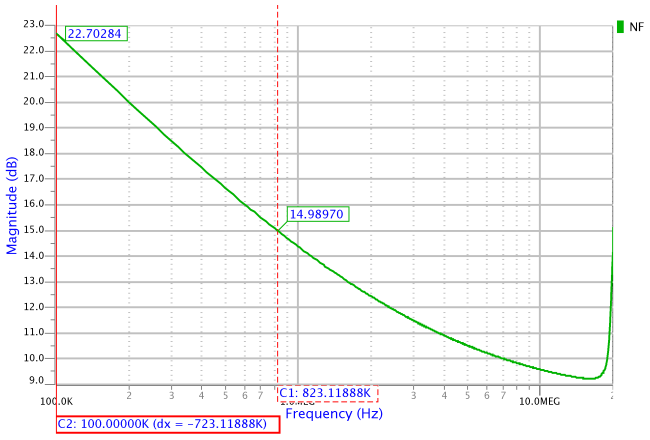

Fig. 8: Noise figure of the mixer, NF = 15dB @ 800kHz

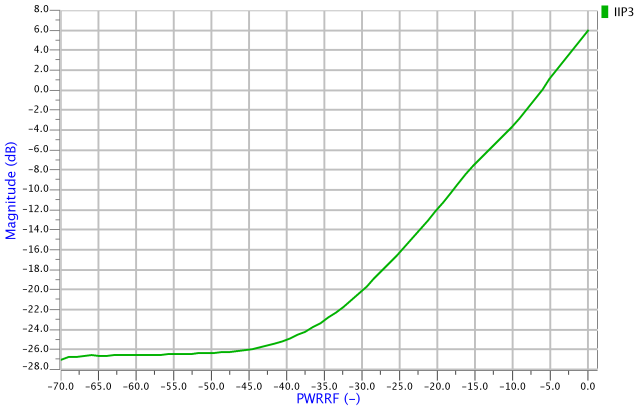

Fig. 11: Input 3^{rd} order Intermodulation Intercept point (IIP3) of the system shown in Fig. 4, IIP3 = -26.0dBm

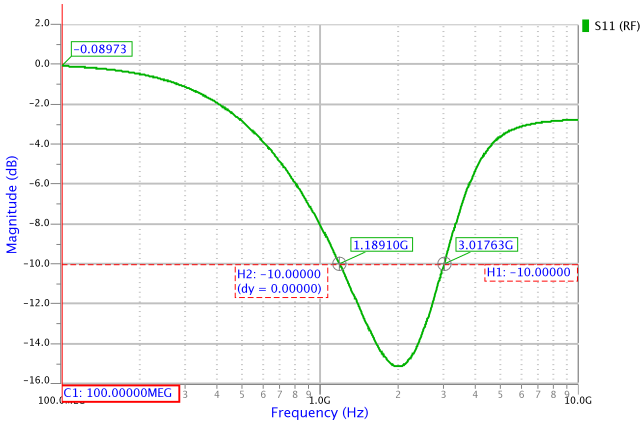

Fig. 9: Return loss at the RF port

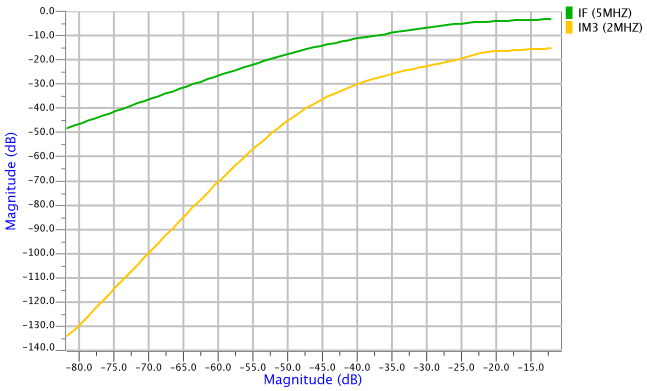

Fig. 12: Plot showing the Fundamental IF component along with intermodulation component of the system shown in Fig. 4

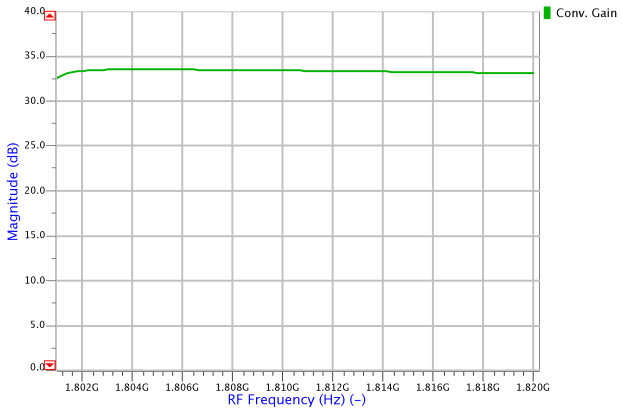

Fig. 10: Conversion gain of the system shown in Fig. 4, Conversion Gain = 33.75dB

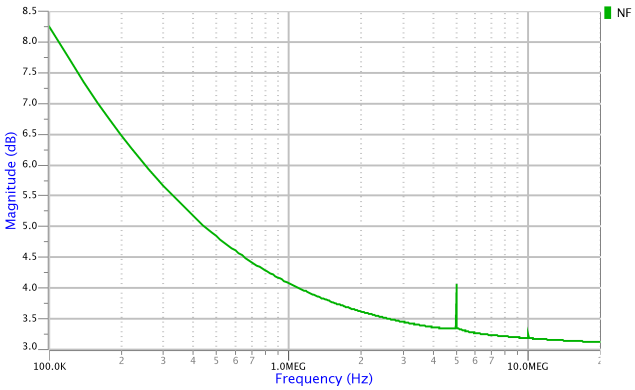

Fig. 13: Noise figure of the system shown in Fig. 4, NF = 4.25dB @ 800kHz

VI. Netlists

A. Netlist.spi (Specific for Noise calculation)

```
* ELDO netlist generated with ICnet by '
    ee18s063' on Sat Apr  6 2019 at
    16:05:35

.CONNECT GROUND 0

*
* Globals.
*
.global GROUND

*
* MAIN CELL: Component pathname : /home/
    ee18s063/Eldo_files/RFIC_EE6320/
    SS_GILBERT_CELL_MIXER_REV1
*
V2 RF GROUND AC 1 IPORT=1 RPORT=50 FOUR
    FUND2 PDBM (1) PWRRF -90.0
L5 RF ground 100n
L6 N$300 N$302 200n
K2 L5 L6 1
R4 VDD OUTP {Rd/2} NOISE=1
M15 N$268 VBIAS GROUND GROUND N_18_MM L
    ={3*Length} W={4*Width} M=5
M6 OUTP VLOP N$246 GROUND N_18_MM L={3*
    Length} W={4*Width} M=20
M5 OUTP VLON N$242 GROUND N_18_MM L={3*
    Length} W={4*Width} M=20
M1 OUTN VLOP N$242 GROUND N_18_MM L={3*
    Length} W={4*Width} M=20
R7 N$310 LO 50 NOISE=1
R1 VDD OUTN {Rd/2} NOISE=1
M2 OUTN VLON N$246 GROUND N_18_MM L={3*
    Length} W={4*Width} M=20
L3 VRFP N$300 Lg
M7 OUTN OUTP VDD VDD P_18_MM L={2*Length}
     W={4*Width} M=20
L4 VRFN N$302 Lg
M8 OUTP OUTN VDD VDD P_18_MM L={2*Length}
     W={4*Width} M=20
V5 IF GROUND IPORT=2 RPORT=50
L7 OUTP OUTN 100u
L8 IF ground 100u
K1 L7 L8 1
R14 VBIAS VRFN 100k NOISE=1
R13 VRFP VBIAS 100k NOISE=1
R12 N$271 VLON 100k NOISE=1
R11 VLOP N$271 100k NOISE=1
R10 VDD N$270 100 NOISE=1
M20 N$271 N$271 GROUND GROUND N_18_MM L
    ={3*Length} W=Width M=5
M19 N$271 VBIAS_P VDD VDD P_18_MM L={2*
    Length} W={4*Width} M=5
M18 VBIAS_P VBIAS_P VDD VDD P_18_MM L={2*
    Length} W={4*Width} M=5
M17 VBIAS_P VBIAS GROUND GROUND N_18_MM L
    ={3*Length} W={4*Width}
+  M=5
M16 N$270 N$271 N$268 GROUND N_18_MM L
    ={3*Length} W={4*Width} M=5
M14 VBIAS VBIAS GROUND GROUND N_18_MM L
    ={3*Length} W={4*Width} M=5
I2 VDD VBIAS DC Ibias
L2 N$307 GROUND Ls
L1 N$306 GROUND Ls
L9 LO ground 200n
L10 VLOP VLON 400n
K3 L9 L10 1
M3 N$242 VRFP N$306 GROUND N_18_MM L={3*
    Length} W={4*Width} M=20
R6 N$307 GROUND Rs NOISE=1
R5 N$306 GROUND Rs NOISE=1
R3 VRFN N$302 Rg NOISE=1
R2 VRFP N$300 Rg NOISE=1
M4 N$246 VRFN N$307 GROUND N_18_MM L={3*
    Length} W={4*Width} M=20
V4 VDD GROUND DC 1.8
V3 N$310 GROUND FOUR FUND1 MA (1) MAGLO
    -90.0
*
.end
```

B. SS_GILBERT_CELL_MIXER_REV1_default_default_nf.cir

```
* Component: /home/ee18s063/Eldo_files/
    RFIC_EE6320/SS_GILBERT_CELL_MIXER_REV1
     Viewpoint: default

.OPTION COMPAT
.INCLUDE "/home/ee18s063/Eldo_files/
    RFIC_EE6320/SS_GILBERT_CELL_MIXER_REV1
    /default/netlist.spi"
.OPTION AEX
.OPTION ENGNOT
.OPTION LIMPROBE=10000.0
.OPTION NOASCII
.EXTRACT DC LABEL = cgs -1*CGS(M3)
.EXTRACT DC LABEL = cgb -1*CGB(M3)
.EXTRACT DC LABEL = gm3 GM(M3)
.EXTRACT DC LABEL = rds3 1/GDS(M3)
.EXTRACT DC LABEL = wt gm3/cgs
.PLOT FSST VDB(IF)
.PLOT FSST VDB(RF)
.EXTRACT FSST LABEL = IF_MAG YVAL(V(IF),
    FUND2-FUND1)
.EXTRACT FSST LABEL = RF_MAG YVAL(V(RF),
    FUND2)
.EXTRACT FSST LABEL = CONV_GAIN IF_MAG/
    RF_MAG
```

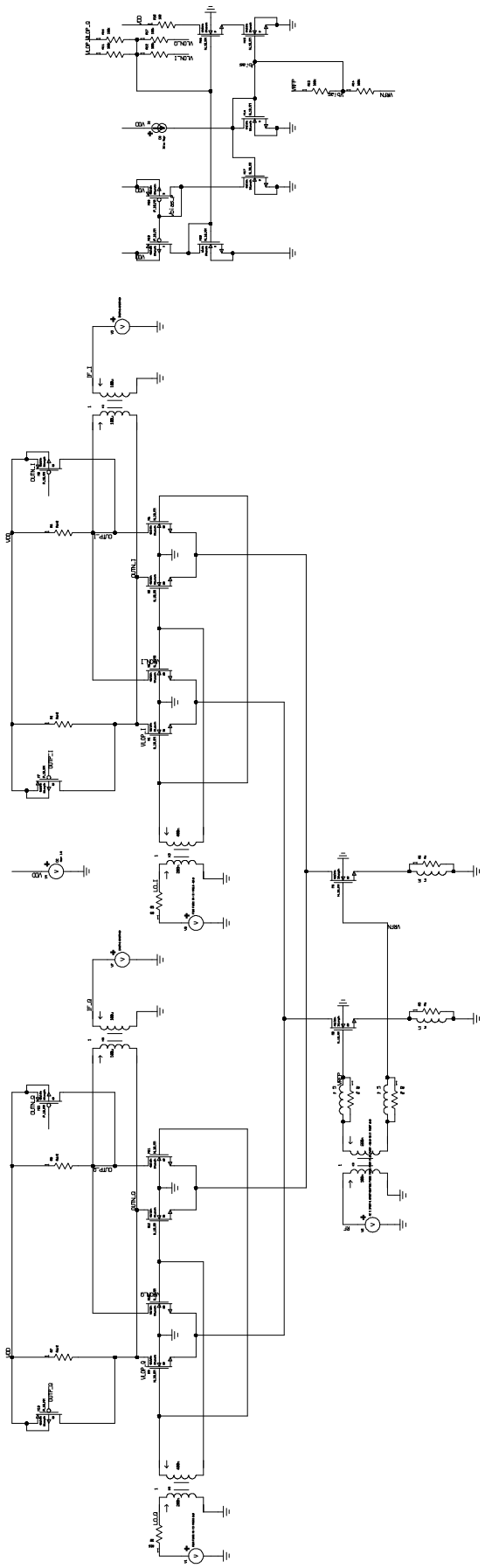

Fig. 14: Pyxis (ELDO) schematic of I-Q Mixer

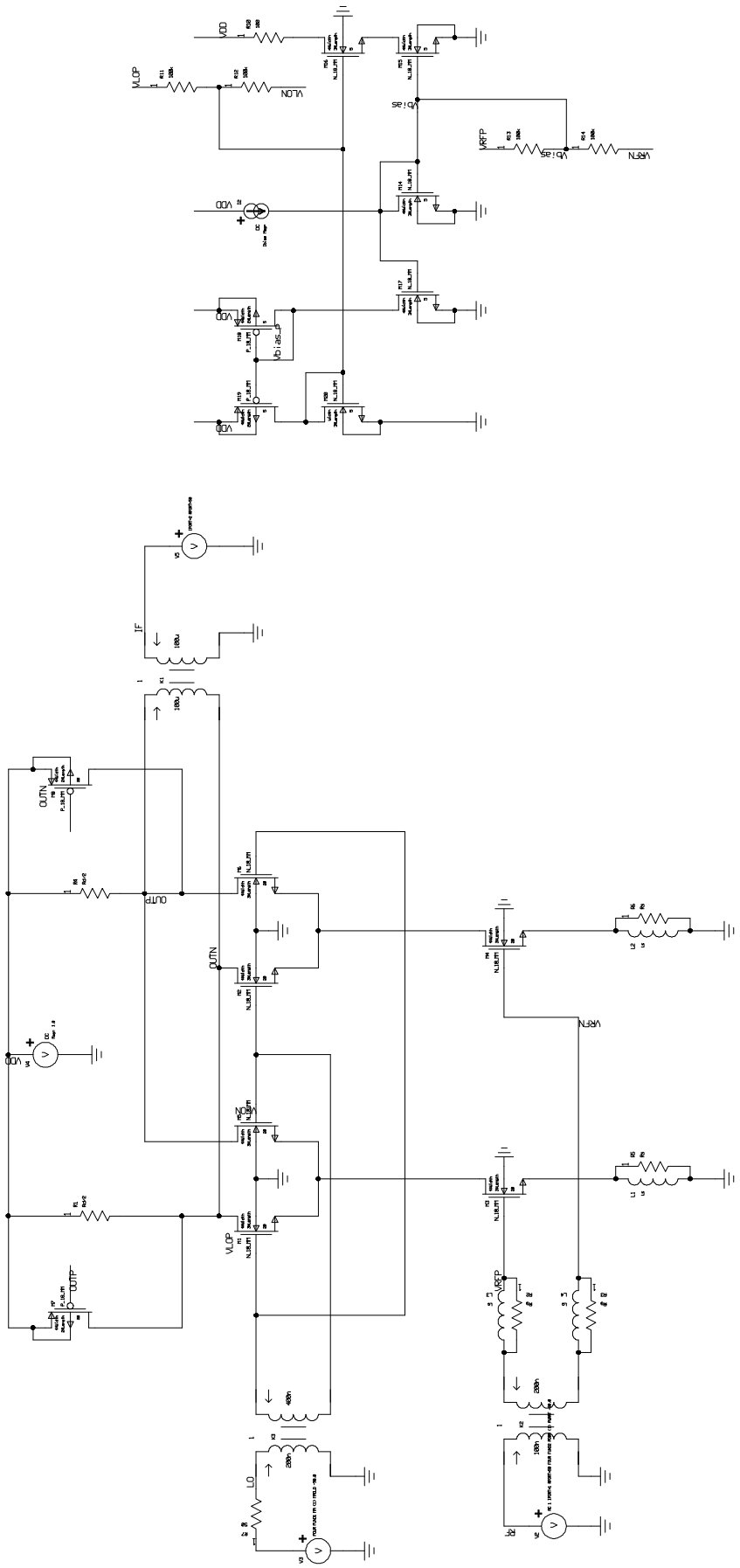

Fig. 15: Pyxis (ELDO) schematic of Mixer

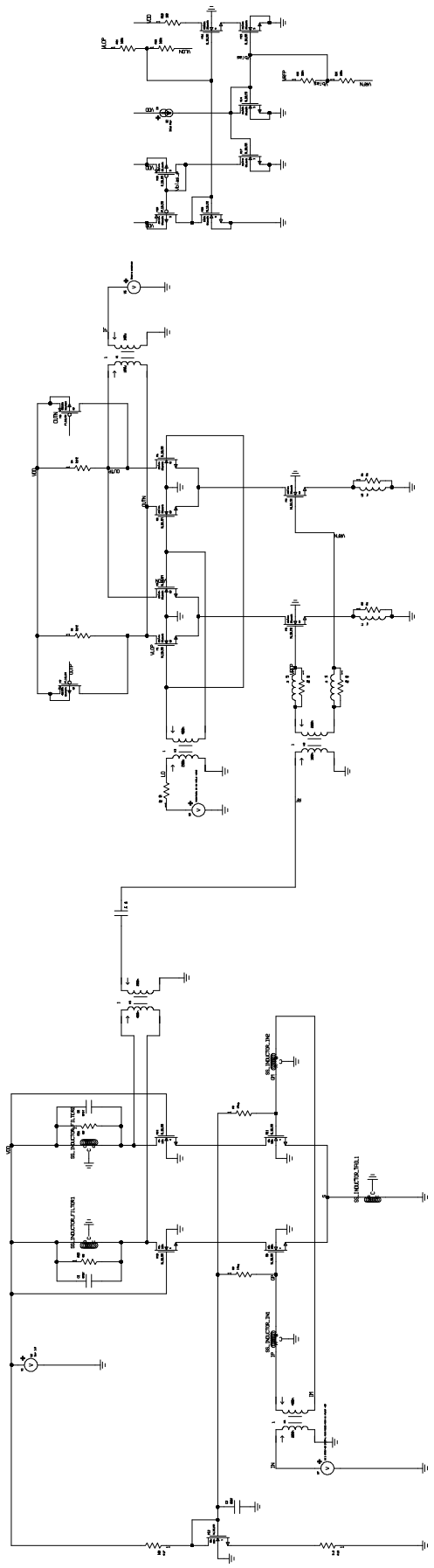

Fig. 16: Pyxis (ELDO) schematic of Mixer preceded by LNA

```
.EXTRACT FSST LABEL = CONV_GAIN_DB DB(
    CONV_GAIN)
.PLOT TSST V(VLOP)
.PLOT TSST V(VLON)
.PLOT TSST V(VRFP)
.PLOT TSST V(VRFN)
.PLOT TSST V(OUTN)
.PLOT TSST V(OUTP)
.PLOT TSST V(RF)
.PLOT TSST V(LO)
.PLOT TSST V(IF)
.EXTRACT DC LABEL = gm7 GM(M7)
.PLOT AC SDB(1,1)
.SNF INPUT=(V2) OUTPUT=(V5)
.PLOT SSTNOISE ONOISE
.PLOT SSTNOISE DB(SNF)
.EXTRACT SSTNOISE LABEL = noise@2MHz yval
    (SNF_MAG,20Meg)
.EXTRACT FSST LABEL = IF_MAG_IM3_2MHZ
    YVAL(V(IF),2*FUND3-FUND2-FUND1)
.EXTRACT FSST LABEL = IF_MAG_IM3_4MHZ
    YVAL(V(IF),2*FUND2-FUND3-FUND1)
.EXTRACT FSST LABEL = IF_MAG_5MHZ YVAL(V(
    IF),FUND2-FUND1)
.EXTRACT FSST LABEL = IF_MAG_6MHZ YVAL(V(
    IF),FUND3-FUND1)
.EXTRACT FSST LABEL = RF_MAG_FUND2 YVAL(V
    (RF),FUND2)
.EXTRACT FSST LABEL = RF_MAG_FUND3 YVAL(V
    (RF),FUND3)
.EXTRACT FSST LABEL = IIP3 PWRRF + (DB(
    IF_MAG_5MHZ) - DB(IF_MAG_IM3_2MHZ))/2
.EXTRACT FSST LABEL = IIP3_ANTILOG 10**(
    IIP3/20)

* - Analysis Setup - DCOP
.OPTION PROBEOP2
.OP

* - Analysis Setup - DC
.DC

* - Analysis Setup - AC
.AC DEC 1000 100Meg 10G

* - Analysis Setup - SST
.SST FUND1=FUND1 NHARM1=5
+ FUND2=FUND2 NHARM2=5
.SAVE SST

* - Analysis Setup - SST Noise
.SSTNOISE V(IF) V2 INPUT_HARM(-1,0) HARM
    (0,0) LIN 1000 100k 20Meg
+ XAXIS=FREQ_SPECTRUM
.PLOT SSTNOISE DB(INOISE)
.PLOT SSTNOISE DB(ONOISE)
.PLOT SSTNOISE DB(AMNOISE)

* --- Global Outputs
.PROBE V SG

* --- Params
.TEMP 27.0
.PARAM Width =10u
.PARAM Length=180n
.PARAM Rd=230
.PARAM MAGLO=0.9
.PARAM FUND1=1.8G
.PARAM FUND2=1.82G
.PARAM PWRRF=-30
.PARAM Ibias=4.5m
.PARAM Cp=16p
.PARAM Ls=1.25n
.PARAM Lg=3n
.PARAM Rs=140
.PARAM Rg=330
.PARAM FUND3=1.806G

* --- Libsetup
.LIB KEY=TT "/home/ee18s063/Eldo_files/
    Models_UMC180/MM180_REG18_V124.lib" TT
```

VII. Conclusions

The I-Q Mixer has been designed successfully in schematic level keeping in mind about all the possible parasitics (inductors). The signal chain from LNA to Mixer is also studied. The comparision between theoretically calculated values and simulated values are presented in Table II. The power consumption is found to be 88mW for Mixer and 156mW for LNA-Mixer system.

References

[1] Tutorial 6 Mixer Steady-State AC Analysis for a Gilbert Cell, ELDO RF User-Manual, Page 322

[2] Mixer Basics Primer, A Tutorial for RF & Microwave Mixers, Ferenc Marki & Christopher Marki, Ph.D., Marki Microwave Inc.

[3] Behzad Razavi. 2011. RF Microelectronics (2nd Edition) (Prentice Hall Communications Engineering and Emerging Technologies Series) (2nd ed.). Prentice Hall Press, Upper Saddle River, NJ, USA