Low Power, Differential Common-Source Low-Noise Amplifier (LNA)

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Abstract—**To design and simulate schematic level Common source cascode LNA using UMC 180nm technology to be operated in 1.7GHz - 1.9GHz.**

Index Terms—**Noise Figure, S-parameters, IIP3, IIP2, SNR, P1dB, Baluns, LNA**

I. INTRODUCTION

In RF Reciever systems, the electronic signal is generated using the transducer (antenna). This electronic signal is picked up by a device called amplifier. The signal may have come from a large distance so, the SNR & power of the signal is very low. The amplifier itself has noise which adds up in the incoming signal and produced at the output. The amplifier cannot distinguish between signal and noise of the incoming signal so it cannot selectively suppress noise of the incoming signal. However one thing that it can do confidently is to add as little noise as possible from its own noise sources. So, the amplifiers having this property of adding very little noise to input signal are called Low Noise Amplifiers (LNAs). The LNA does not increase the SNR of the incoming signal but tries to atleast retain it without degrading it from its own noise sources. However this increase in gain helps the output signal to tolerate subsequent noisy devices like mixers.

II. REQUIREMENTS

Sr. No	Property	Value
1.	R_{in}	50Ω (single ended)
		100Ω (differential)
2.	R_{out}	50Ω (single ended)
		100Ω (differential)
3.	NF	$\leq 1.5dB$
4.	IIP_3	$\geq -10dBm$
5.	Supply Voltage	1.8V
6.	Power	Minimum
7.	S_{11}	$\leq -10dB$
8.	S_{12}	$\leq -50dB$
9.	S_{21}	$\geq 15dB$
10.	S_{22}	$\leq -10dB$
11.	Frequency	$1.8GHz$
12.	Band	$1.7GHz - 1.9GHz$

TABLE I: Requirements of the LNA

III. TOPOLOGY

A. LNA

There are 3 basic topologies for implementation of the LNA.

1) CG Amplifier: This topology effectively provides gain of $g_m R_D$ which is usable for amplification purpose. However the input impedance is dependent on the output impedance which is undesirable.

$$R_{in} = \frac{R_D + r_o}{1 + g_m r_o}$$

This also leads to high S_{12}. To mitigate this we can cascode it with another common-gate amplifier. This leads to an input impedance of,

$$R_{in} = \frac{R_D + r_{o2} + r_{o1} + g_{m2}r_{o1}r_{o2}}{(1 + g_{m1}r_{o1})(1 + g_{m2}r_{o2})}$$

This is still dependent on $g_m r_o$ whether it is very high compared to 1. In our case it is found to be $\simeq 18.86V/V$. This seems sufficient value to be considered for the fact $g_m r_o \gg 1$. But we will search for better alternative.

2) CD Amplifier: This topology does not provide gain ≥ 1 so, this cannot be used here.

3) CS Amplifier: This topology as CG amplifier provides gain of $g_m R_D$. But unlike the CG amplifier, it provides input impedance which is independent of the output impedance. So, the design of S_{22} can be done independently which eases the design process. However due to parasitic capacitance C_{gd} reverse isolation S_{12} is not good (it's around $-24.3dB$). To decrease it (S_{12}) further we need to add cascode CG amplifier. This addition improved the S_{12} (now $-49.30dB$, see Fig. 6). This is still not very low because of low r_{ds} at high W. However cascode devices M2 and M4 has helped to reduce the amplitude of $V_{S,M2}$ and $V_{S,M4}$ and subsequently the signal coupled in input port using $C_{gd,M1}$ and $C_{gd,M3}$ respectively. This also helps to increase the IIP_3 because drain of M1 and M3 are subjected to lower voltage swings keeping them out of any voltage saturation levels.
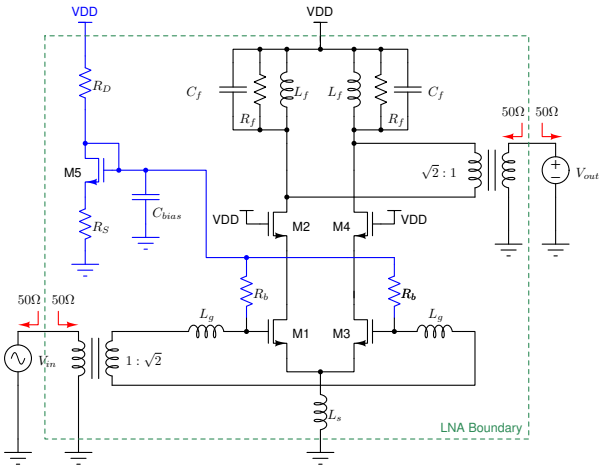
Fig. 1: Differential Common-Source LNA Schematic

B. IIP2

In single ended amplifiers, the 2nd order harmonic is generated due to second order non-linearity. Since it is even term we can get rid of this using a differential amplifier topology. This allows to cancel the even order terms and retain odd order terms. However even after deploying differential topologies the IIP2 may not be cancelled properly because of mismatches. So, in schematic simulation level the mismatches are not any concern.

C. Baluns

Mutually coupled ideal inductors have been used as baluns. These are nothing but transformers. The coupling coefficient (k) has been set to 1 (in case of ideal transformer). Turns ratio for input is set to $1 : \sqrt{2}$ and for output it is set to $\sqrt{2} : 1$. Inductance (L) have been set arbitrarily high.

D. Inductor model

In integrated circuit, an inductor fabricated comes with distributed resistors and capacitors which reduces the Q of the inductor and also decreases the self resonant frequency. We exploit this feature to increase the bandwidth, however the exact value of the inductor parasitics are subject rigorous simulation followed by silicon interations ! However using [1] & [2] we have estimated the inductor parasitics. Every inductor used in the project (Fig. 1) except the baluns are modelled using Fig. 2.

IV. DESIGN

The LNA can be considered as a 2 port network. We talk about S-parameters in high frequency 2-port networks because the time domain operations on such circuits is expensive (infeasible too!). The design started with the output S_{22} parameter because it is independent of the other parameters. It was required to be $\leq -10dB$ in entire band. The differential R_{out} has to be 100Ω for minimum S_{22}. The output impedance of the cascode part is calculated to be $\gg 100\Omega$. So the output gain (S_{21}) predominantly depend upon R_{out} (assuming all

other ports are matched; the output small signal impedance of cascode is very high). So, at proper matching (input and output both) the gain is $g_m R_{out} Q_{in}/4$. The Quality factor Q_{in} is multiplied because input is a series resonant circuit. The input is taken from Gate-Source capacitor (C_{gs}), so the effective input voltage is $Q_{in}V_{in}$. We can estimate the Q_{in} by simulation (it is a complex network) by as shown in Fig. 4,

$$Q_{in} = \frac{V_{gs}(\omega_o)}{V_{in}(\omega_o)}$$

For starting the process of iteration, we start by taking $Q_{in} = 5$.
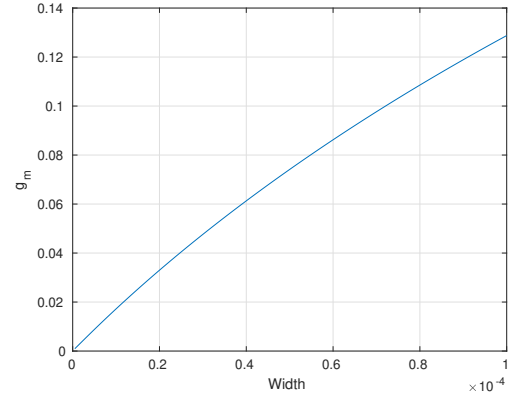

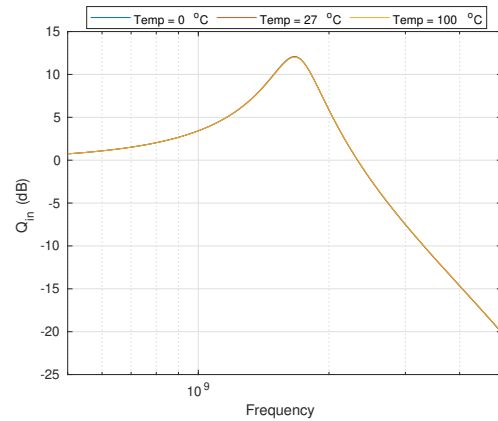Fig. 3: g_m vs. $width$ of MOSFET at $V_{gs} = 1.0V$

Fig. 4: Q_{in} vs. $Frequency$ of the LNA

Required $S_{21} \geq 15dB$, implies required gain of $5.62V/V$. This implies

$$g_m = \frac{5.62 \times 4}{100 \times 5} = 44.96mA/V$$

From here we can estimate the approximate width and length of the MOSFETs using $g_m vs. W$ curve (obtained through simulation, Fig. 3). It is found that for obtaining $g_m = 44.96mA$ using a single multiplier it exceeds $100um$ of length which is restricted. So, we choose multiplier of 4 to divide the

effective width by 4. Now the (W) is coming to around $28um$ for each transistor, for $(L) = 180nm$ $(V_g = 1.00V)$. After doing certain iterations (6-7) we arrive at $W = 60um$ and $R_{out} = 160\Omega$, where parameters $(S_{11},S_{12},S_{21},S_{22})$ are found to be as per requirements. However Noise Figure (NF) is still $2.37dB$. Using the relation for Noise Figure in Cascode CS amplifier [3],

$$NF = 1 + g_m R_s \gamma \left(\frac{\omega_o}{\omega_T}\right)^2 + \frac{4R_s}{R_f}\left(\frac{\omega_o}{\omega_T}\right)^2$$

We know,

$$\omega_T = \frac{g_m}{C_{gs}}$$

So, we observe that changing g_m or V_{ov} no longer changes the noise figure significantly. However increasing R_b from $2k\Omega$ to $100k\Omega$ reduces NF from $2.37dB$ to $2.15dB$. The IIP_3 is found to be within requirements without any special efforts.

V. RESULTS

Fig. 2: Inductor with parasitics

Sr. No	Parameters	Values
1.	S_{11}	$-11.89dB$, 1.8GHz
		$-11.17dB$, 1.7GHz
		$-10.24dB$, 1.9GHz
2.	S_{22}	$-17.95dB$, 1.8GHz
		$-16.70dB$, 1.7GHz
		$-17.95dB$, 1.9GHz
3.	S_{12}	$-49.30dB$, 1.8GHz
		$-49.32dB$, 1.7GHz
		$-49.55dB$, 1.9GHz
4.	S_{21}	$15.91dB$, 1.8GHz
		$15.24dB$, 1.9GHz
		$16.04dB$, 1.7GHz
5.	NF	$2.15dB$, 1.8GHz
6.	IIP_3	$0.7dBm$
7.	$P1dB$	$-14.29dBm$
8.	$Power$	$68mW$

TABLE II: Result table

Fig. 6: Reverse Isolation (S_{12}) vs Temperature

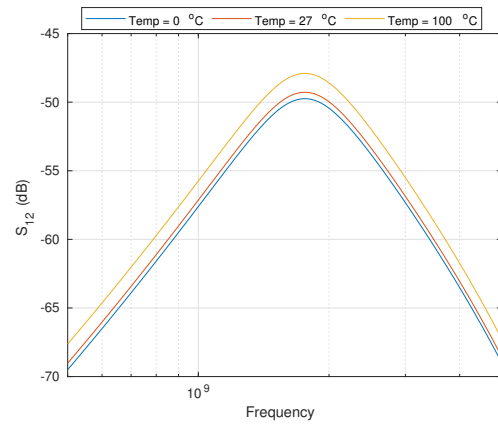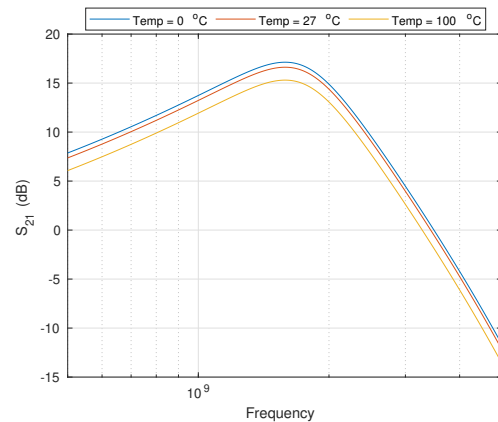Fig. 5: Input Return Loss (S_{11}) vs Temperature
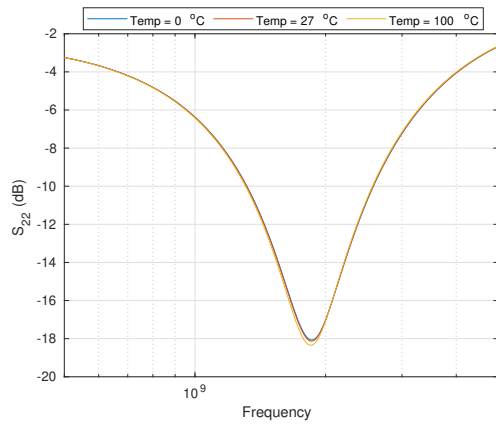

Fig. 7: Forward Gain (S_{21}) vs Temperature

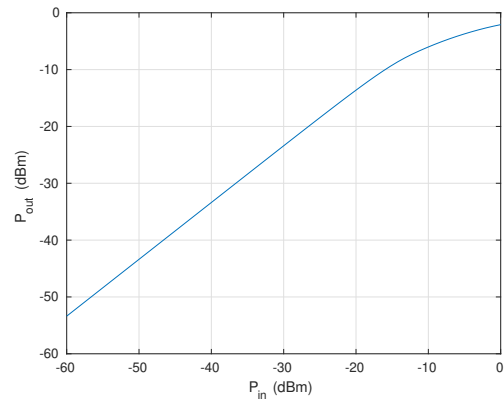Fig. 8: Output Return Loss (S_{22}) vs Temperature

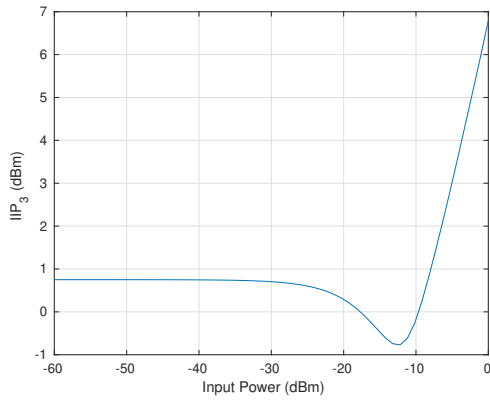Fig. 11: Fundamental Output power vs. Input power of the LNA
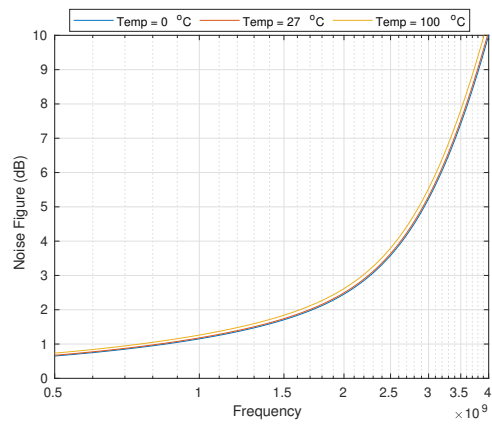

Fig. 9: IIP_3 vs. Input power

Fig. 12: Noise figure vs. Frequency of the LNA
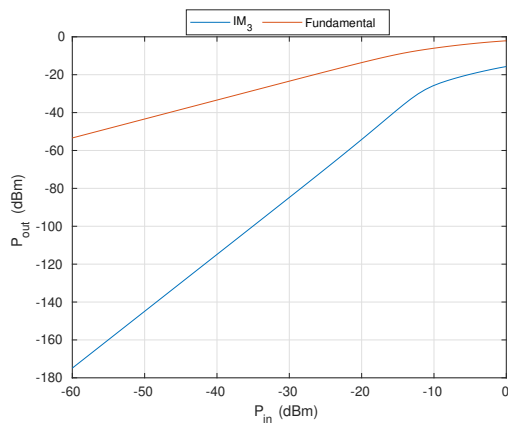
VI. NETLISTS

A. *netlist.spi*

```
* ELDO netlist generated with ICnet by '
    ee18s063' on Sun Mar 17 2019 at
    08:30:42

.CONNECT GROUND 0

*
*  Globals.
*
.global GROUND

*
* Component pathname : /home/ee18s063/
    Eldo_files/RFIC_EE6320/
    SS_INDUCTOR_FILTER
*
.subckt SS_INDUCTOR_FILTER   B C A

C2 N$4 A 200f
```


Fig. 10: IM_3 and Fundamental Output power vs. Input power of the LNA

```
C5 C N$5 1f
R3 C N$5 35.27 NOISE=1
C4 C N$4 1f
R2 C N$4 35.27 NOISE=1
C3 N$5 B 200f
C1 A B 28f
R1 N$1 B 7.5 NOISE=1
L1 A N$1 5n
.ends SS_INDUCTOR_FILTER


*
* Component pathname : /home/ee18s063/
    Eldo_files/RFIC_EE6320/SS_INDUCTOR_IN
*
.subckt SS_INDUCTOR_IN  B C A

R4 A B 3500 NOISE=1
C5 C N$5 1f
R3 C N$5 40 NOISE=1
C4 C N$4 1f
R2 C N$4 40 NOISE=1
C3 N$5 B 337f
C2 N$4 A 337f
C1 A B 28f
R1 N$1 B 16.5 NOISE=1
L1 A N$1 10.5n
.ends SS_INDUCTOR_IN


*
* Component pathname : /home/ee18s063/
    Eldo_files/RFIC_EE6320/
    SS_INDUCTOR_TAIL
*
.subckt SS_INDUCTOR_TAIL  B C A

R4 A B 500 NOISE=1
C5 C N$5 1f
R3 C N$5 35.27 NOISE=1
C4 C N$4 1f
R2 C N$4 35.27 NOISE=1
C3 N$5 B 85f
C2 N$4 A 85f
C1 A B 28f
R1 N$1 B 7.5 NOISE=1
L1 A N$1 2n
.ends SS_INDUCTOR_TAIL


*
* MAIN CELL: Component pathname : /home/
    ee18s063/Eldo_files/RFIC_EE6320/
    SS_CS_LNA_REV5
*
V3 N$8 GROUND DC 1.8
M1 N$2 GP S GROUND N_18_MM L=L W=W M=4
R3 N$38 GP 1Meg NOISE=1
V1 IN GROUND AC 1 RPORT=50 IPORT=1 FOUR
```

```
     1.8G 1.801G PDBM (1,0) PWR
+    −90 (0,1) PWR −90
L1 N$15 N$10 400n
L2 OUT ground 200n
K2 L1 L2 1
M5 N$38 N$38 N$41 GROUND N_18_MM L=L W=
    Wbias M=1
L3 IN ground 200n
L4 IP IM 400n
K1 L3 L4 1
X_SS_INDUCTOR_FILTER1 N$8 GROUND N$10
    SS_INDUCTOR_FILTER
X_SS_INDUCTOR_FILTER2 N$15 GROUND N$8
    SS_INDUCTOR_FILTER
C3 N$38 GROUND 500f
X_SS_INDUCTOR_IN2 IM GROUND GM
    SS_INDUCTOR_IN
X_SS_INDUCTOR_TAIL1 S GROUND GROUND
    SS_INDUCTOR_TAIL
V2 OUT GROUND RPORT=50 IPORT=2
X_SS_INDUCTOR_IN1 GP GROUND IP
    SS_INDUCTOR_IN
R5 N$38 GM 1Meg NOISE=1
R4 N$38 N$8 100 NOISE=1
M2 N$10 N$8 N$2 GROUND N_18_MM L=L W=W M
    =4
R2 N$8 N$15 80 NOISE=1
C2 N$8 N$15 875f
R1 N$8 N$10 80 NOISE=1
C1 N$8 N$10 875f
R6 GROUND N$41 3.5 NOISE=1
M4 N$15 N$8 N$12 GROUND N_18_MM L=L W=W M
    =4
M3 N$12 GM S GROUND N_18_MM L=L W=W M=4
*
.end
```

B. SS_CS_LNA_REV5_default_1_default.cir

```
* Component: /home/ee18s063/Eldo_files/
    RFIC_EE6320/SS_CS_LNA_REV5 Viewpoint:
    default_1

.OPTION COMPAT
.INCLUDE "/home/ee18s063/Eldo_files/
    RFIC_EE6320/SS_CS_LNA_REV5/default_1/
    netlist.spi"
.OPTION AEX
.OPTION ENGNOT
.OPTION LIMPROBE=10000.0
.OPTION NOASCII
.PLOT AC SDB(1,1)
.PLOT AC SDB(2,2)
.PLOT AC SDB(2,1)
.PLOT AC SDB(1,2)
.EXTRACT DC LABEL = cgs1 −1*CGS(M1)
.EXTRACT DC LABEL = cgb1 −1*CGB(M1)
```

.EXTRACT DC LABEL = gm1 GM(M1)
.EXTRACT DC LABEL = gm2 GM(M2)
.EXTRACT DC LABEL = gds1 GDS(M1)
.EXTRACT DC LABEL = gds2 GDS(M2)
.EXTRACT DC LABEL = rds1 1/gds1
.EXTRACT DC LABEL = rds2 1/gds2
.EXTRACT DC LABEL = RDS rds2*rds1*gm1
.EXTRACT DC LABEL = wt gm1/(cgs1+cgb1)
.EXTRACT DC LABEL = id ID(M1)
.DEFWAVE GAIN=VDB(OUT)−VDB(IN)
.PLOT AC W(GAIN)
.DEFWAVE QDB = VDB(GP)−VDB(IP)
.PLOT AC W(QDB)
.SNF INPUT=(V1) OUTPUT=(V2)
.PLOT NOISE DB(SNF) DB(NFMIN)
.EXTRACT NOISE LABEL = NFmax YVAL(SNF_DB
   ,1.9G)
.PLOT FSST V(OUT)
.EXTRACT FSST LABEL = POUT_2W2_W1 YVAL(V(
   OUT),1.799G)
.EXTRACT FSST LABEL = POUTDBM_2W2_W1 DB(
   POUT_2W2_W1)
.EXTRACT FSST LABEL = POUT_W2 YVAL(V(OUT)
   ,1.8G)
.EXTRACT FSST LABEL = POUTDBM_W2 DB(
   POUT_W2)
.EXTRACT FSST LABEL = POUT_W1 YVAL(V(OUT)
   ,1.801G)
.EXTRACT FSST LABEL = POUTDBM_W1 DB(
   POUT_W1)
.EXTRACT FSST LABEL = POUT_2W1_W2 YVAL(V(
   OUT),1.802G)
.EXTRACT FSST LABEL = POUTDBM_2W1_W2 DB(
   POUT_2W1_W2)
.EXTRACT FSST LABEL = IIP3 ((POUTDBM_W1 −
   POUTDBM_2W1_W2)/2 + PWR)
.EXTRACT FSST LABEL = IIP3_ANTILOG 10**(
   IIP3/20)
.EXTRACT DC LABEL = POWER −1.8*I(V3)
.EXTRACT AC LABEL = VGS V(GP)
* Use for determining P1dB with sweep in
   input power
.EXTRACT SWEEP XCOMPRESS(MEAS(POUTDBM_W1)
   ,1.0)
.EXTRACT SWEEP COMPRESS(MEAS(POUTDBM_W1)
   ,1.0)

* − Analysis Setup − DCOP
.OPTION PROBEOP2
.OP

* − Analysis Setup − DC
.DC

* − Analysis Setup − AC
.AC DEC 2000 500Meg 5G

* − Analysis Setup − AC Noise
.NOISE V(OUT) V1 10 NOMOD=0

* − Analysis Setup − SST
.SST FUND1=1.8G NHARM1=5
+ FUND2=1.801G NHARM2=5

* ——— Global Outputs
.PROBE V SG

* ——— Params
.TEMP 27.0
.PARAM W=60u
.PARAM L=180n
.PARAM PWR=−50
.PARAM Wbias=50u
.STEP PARAM W 500n 100u LIN 100

* ——— Libsetup
.LIB KEY=TT "/home/ee18s063/Eldo_files/
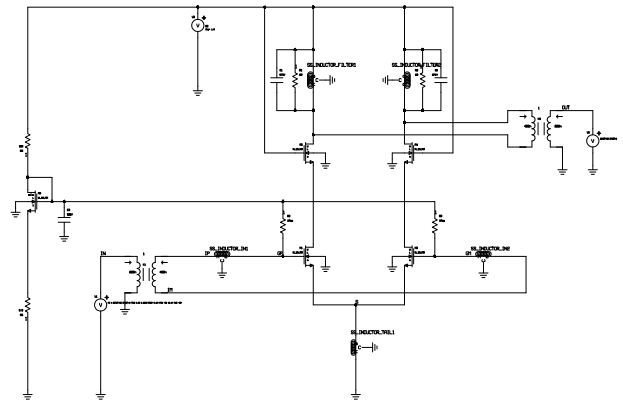   Models_UMC180/MM180_REG18_V124.lib" TT
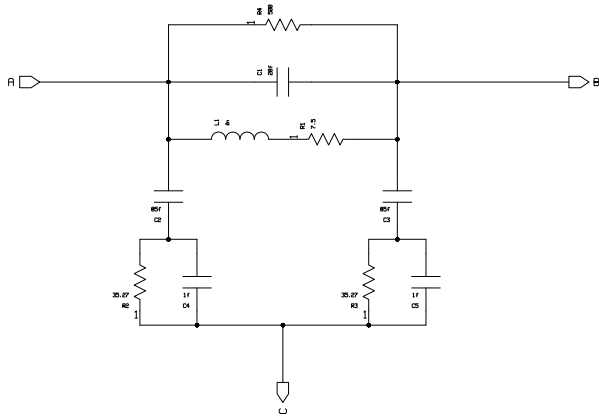

Fig. 13: Schematic of Netlist mentioned in *netlist.spi*

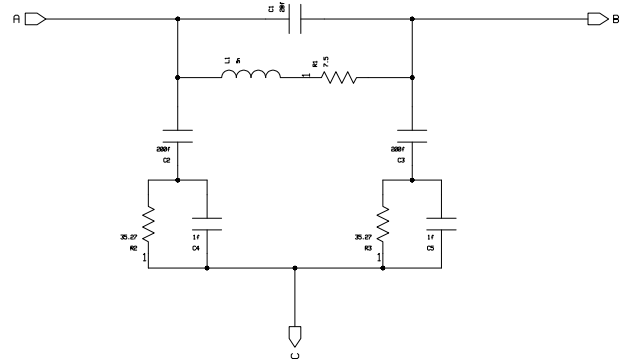Fig. 14: Schematic of Inductor for subcircuit
$SS\_INDUCTOR\_TAIL$

Fig. 16: Schematic of Inductor for subcircuit
$SS\_INDUCTOR\_FILTER$

VII. Conclusions

The LNA has been designed successfully in schematic level keeping in mind about all the possible parasitics (inductors). However the Noise figure ($2.15dB$) is higher than specified ($1.5dB$). All other parameters are well satisfying the specifications. The power consumption is found to be 68mW.

References

[1] Yue, C. P., & Wong, S. S. (2000). Physical modeling of spiral inductors on silicon. IEEE Transactions on electron devices, 47(3), 560-568.
[2] C. Patrick Yue. On-Chip Spiral Inductors for Silicon-Based Radio-Frequency Integrated Circuits (Presentation)
[3] Behzad Razavi. 2011. RF Microelectronics (2nd Edition) (Prentice Hall Communications Engineering and Emerging Technologies Series) (2nd ed.). Prentice Hall Press, Upper Saddle River, NJ, USA, Page-316
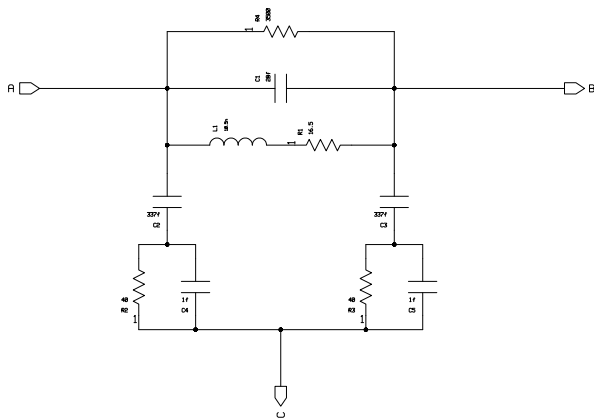
Fig. 15: Schematic of Inductor for subcircuit
$SS\_INDUCTOR\_IN$