

EE5320 - Analog Integrated Circuit Design

Assignment - 6 - Report

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1 Problem 1

1.1 a

Assuming First order system for following reasons :

1. To ensure monotonic behavior of the transient response.
2. To simplify the problem as analysis of first order system is easy.
3. The open loop amplifier would be dominant pole compensated (for stabilisation) to mimic a first order system (even though it has many poles and zeros).

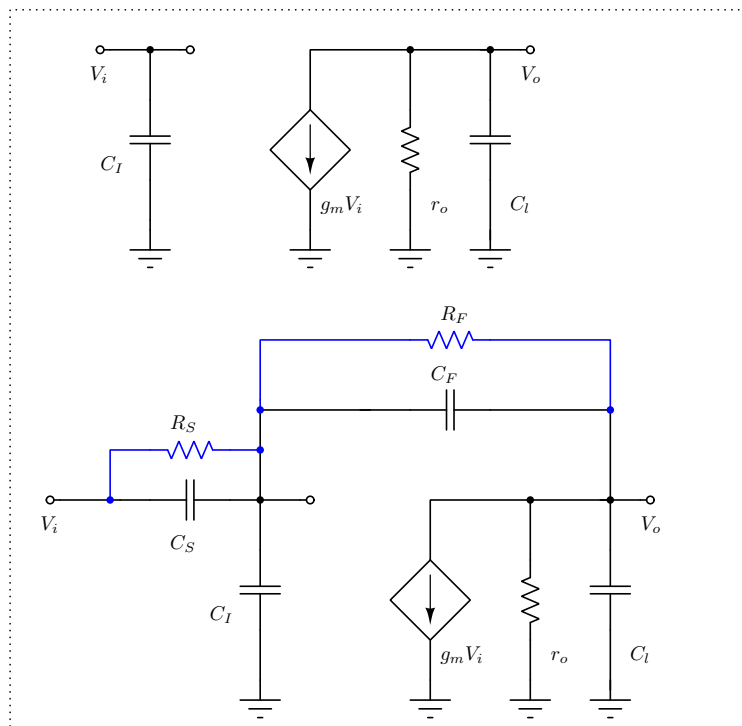


Figure 1: Op-amp model and closed loop Op-Amp (Differential Half-circuit); Components marked in blue are bias resistors having very high value ($R_F = 40\text{M}$, $R_S = 10\text{M}$), these are not considered in the analysis below.

Closed loop transfer function of the system (of differential half-circuit) :

Model for open loop amplifier,

$$\frac{V_o(s)}{V_i(s)} = -\frac{A_o}{1 + sr_o C_l} \quad (1)$$

Amplifier in closed loop,

$$\frac{V_o(s)}{V_i(s)} = -A'_o \frac{1 - s/z_1}{1 + s/p_1} \quad (2)$$

where,

$$A'_o = \frac{C_S}{C_F} \frac{A_o \beta}{A_o \beta + 1} \quad (3)$$

$$\beta = \frac{C_F}{C_I + C_S + C_F} \simeq 0.2 \quad (4)$$

$$p_1 = \frac{g_m + 1/r_o \beta}{C_S + C_I + C'_l + \frac{C'_l}{C_F} (C_S + C_I)} \quad (5)$$

$$\simeq \frac{g_m}{C_S + C_I + \frac{C_l C_S}{C_F}} \quad \because (r_o \beta \gg g_m \ \& \ C'_l \sim C_l) \quad (6)$$

$$z_1 = \frac{g_m}{C_F} \quad (7)$$

Step response

$$V_o(t) = V_i A'_o \left(1 - \left(1 + \frac{p_1}{z_1} \right) e^{-p_1 t} \right) u(t) \quad (8)$$

1.2 b

1.2.1 Finding C_F

Required Closed loop Gain = $-4V/V$

$$\frac{-C_S}{C_F} = -4 \quad (9)$$

$$\therefore C_S = 2pF \quad (10)$$

$$\therefore C_F = 0.5pF \quad (11)$$

1.2.2 Static error

$$\epsilon_s = |V_o(\infty)_{ideal} - V_o(\infty)_{actual}| \quad (12)$$

where,

$$V_o(\infty)_{ideal} = -\frac{C_S}{C_F} V_i \quad (13)$$

$$\therefore \epsilon_s = \frac{C_S}{C_F} V_i \frac{1}{A_o \beta + 1} \quad (14)$$

$$\therefore \epsilon_s \leq 800 \mu V \quad (15)$$

$$C_S = 2pF \quad (16)$$

$$C_F = 0.5pF \quad (17)$$

$$V_i = 300mV \quad (18)$$

$$\beta = 0.2 \quad (19)$$

$$\implies A_o \geq 7495V/V \quad (20)$$

We will try to design for much higher A_o , so that condition for dynamic error meet successfully.

(21)

1.2.3 Dynamic error

$$\epsilon_d(t_s) = |V_o(\infty) - V_o(t_s)| \quad (22)$$

$$\epsilon_d(t_s) = A'_o V_i \left(1 + \frac{p_1}{z_1}\right) e^{-p_1 t_s} \quad (23)$$

where t_s is required settling time (= 5 ns)

$$\frac{p_1}{z_1} \simeq \frac{C_F}{C_S + C_l + \frac{C_l C_S}{C_F}} \quad (24)$$

$$= \frac{0.5p}{0.5 + 2p + \frac{2p \cdot 2p}{0.5p}} = \frac{1}{21} \quad (25)$$

Required settling error = 1/15 % (800 uV/1200 mV), assuming loop gain is sufficiently high

$$\frac{1}{1500} = \left(1 + \frac{1}{21}\right) e^{-p_1 \cdot 5ns} \quad (26)$$

$$p_1 = \frac{7.36}{5ns} \quad (27)$$

$$p_1 = 1.47 \text{ Grad/s} \quad (28)$$

Expected 3-dB frequency of loop gain curve = 234 MHz (1.47/(2 π)Grad/s). Hence 3-dB bandwidth (ω_p) of the op-amp alone, (assuming $A_o = 1 \times 10^8$)

$$\omega_p = \frac{1.47}{1 + 1 \times 10^5 \times 0.2} \times 10^9 \text{ rad/s} \quad (29)$$

$$= 11.7 \text{ KHz} \quad (30)$$

Required unity gain frequency of the op-amp (open-loop model) is (= $f_p A_o$),

$$f_{ugb} = 1.17 \text{ GHz} \quad (31)$$

1.3 c

1.3.1 Folded Cascode Stage : Topology and Transistor sizing

We are using Folded cascode stage (rather than telescopic cascode) because it has better input common mode range and higher output swing limits. These properties allows the transistors to operate in saturation region. Also replicas of this amplifier with slight modification can be used for gain boosting (which increases the gain by power of 2). Cascode amplifiers have used to increase output impedance of the transistors. We require much higher gain that is why we have used gain boosting.

Finding g_{m1} (refer Fig. 5 considering half circuit only),

$$\frac{g_{m1}}{C_L} = \frac{g_{m1}}{2pF + 0.4pF} = 2\pi \times 1.17 \text{ GHz} \quad (32)$$

$$\implies g_{m1} = 17.52 \text{ mA/V} \quad (33)$$

g_{m1} refers to transconductance of transistors M2 and M3 in Fig. 5

DC gain of the amplifier is,

$$A_{DC} = g_{m1} r_o \quad (34)$$

$$\therefore r_o = A_{boost} \cdot g_{m9} \cdot r_{ds9} \cdot r_{ds11} \quad (35)$$

and the boosting amplifier is made from similar op-amp having approximately same DC Gain,

$$A_{boost} = g_{m1} \cdot g_{m9} \cdot r_{ds9} \cdot r_{ds11} \quad (36)$$

$$\therefore A_{DC} = \frac{(g_{m1} \cdot g_{m9} \cdot r_{ds9} \cdot r_{ds11})^2}{2} \quad (37)$$

Required A_{DC} is 10^5

$$\therefore g_{m1} \cdot g_{m9} \cdot r_{ds9} \cdot r_{ds11} = 447 \text{ V/V} \quad (38)$$

Let's allocate $g_{m1} r_{ds11} = 21.14 \text{ V/V}$ and $g_{m9} r_{ds9} = 21.14 \text{ V/V}$

$$V_{DS9} = 1.1 \text{ V} - 0.2 \text{ V} = 0.9 \text{ V} \quad (39)$$

From NMOS characteristic curves (Gain vs. V_{DS}) in Assignment 3 (refer Fig. 3), we observe that for size $2\mu\text{m}/180\text{nm}$, we get sufficient gain of 25V/V for $V_{DS} = 0.9\text{V}$

$$\therefore \left(\frac{W}{L}\right)_9 = \frac{2u}{0.18u} \quad (40)$$

The PMOS transistor ($M7$) is having $V_{DS} = 0.5\text{V}$ so we have to slightly increase the width to get more $g_m r_{ds}$ (refer Fig. 5 and Fig. 2).

$$\therefore \left(\frac{W}{L}\right)_7 = \frac{10u}{0.18u} \quad (41)$$

The size (Gain) of transistor $M7$ should compensate the decrease in r_{ds} of much bigger sized $M5$. So, the actual size may be larger. For first order analysis $g_m r_{ds}$ does not depend on number of multipliers, so we kept the multipliers uniform with transistors in series with them.

(42)

1.3.2 Common Source Stage : Transistor sizing

The second stage is added primarily because of the swing limitations of the first stage (Folded Cascode). Swing limitation in Folded Cascode is less stringent than in Telescopic Cascode. The second stage (CS source single stage amplifier) provides satisfactory gain ($\sim 15\text{V/V}$), thus the output swing at the first stage is reduced by the gain of the second stage. The V_{DS} of both the PMOS ($M12$) and NMOS ($M14$) is 0.9V . So we follow the previous sizes to get similar gain.

$$\left(\frac{W}{L}\right)_{12} = \frac{10u}{0.18u} \quad (43)$$

The $M14$ is a current source so we have used twice the length (and width) of NMOS ($M9$),

$$\left(\frac{W}{L}\right)_{14} = \frac{4u}{0.36u} \quad (44)$$

All these device sizes may change a bit during simulation for fine tuning. We should however make effort to increase the g_{m12} to satisfy the condition for atleast 45° phase margin.

$$g_{m2} \geq \frac{C_L}{C_c} g_{m1} \quad (45)$$

We observe that $\beta = 0.2$ with open loop gain may provide too much phase margin, which in turn can increase the rise time. Therefore in this assignment we have tried to make Loop Gain stability than the open loop stability. We can observe that the open loop (without β) is unstable (refer Fig. 11) while loop gain (with β) is stable with phase margin 73° (ref Fig. 10).

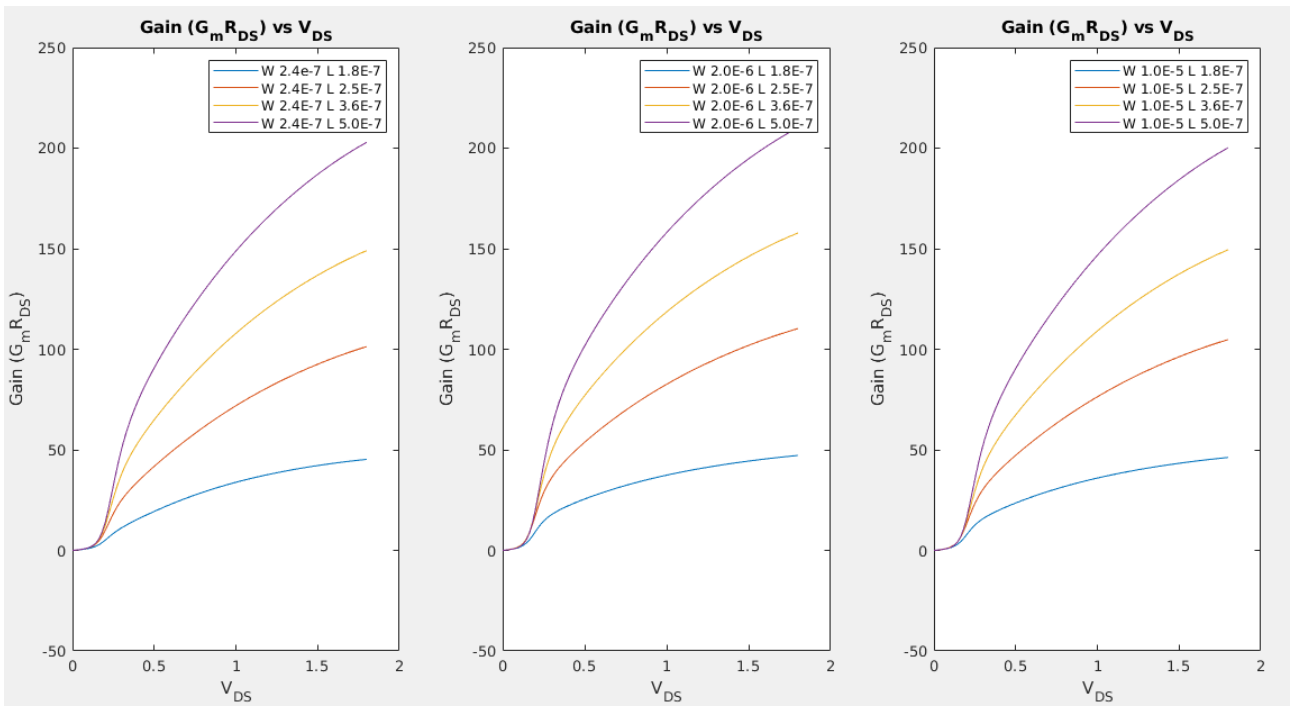


Figure 2: Plot of PMOS Gain vs V_{DS}

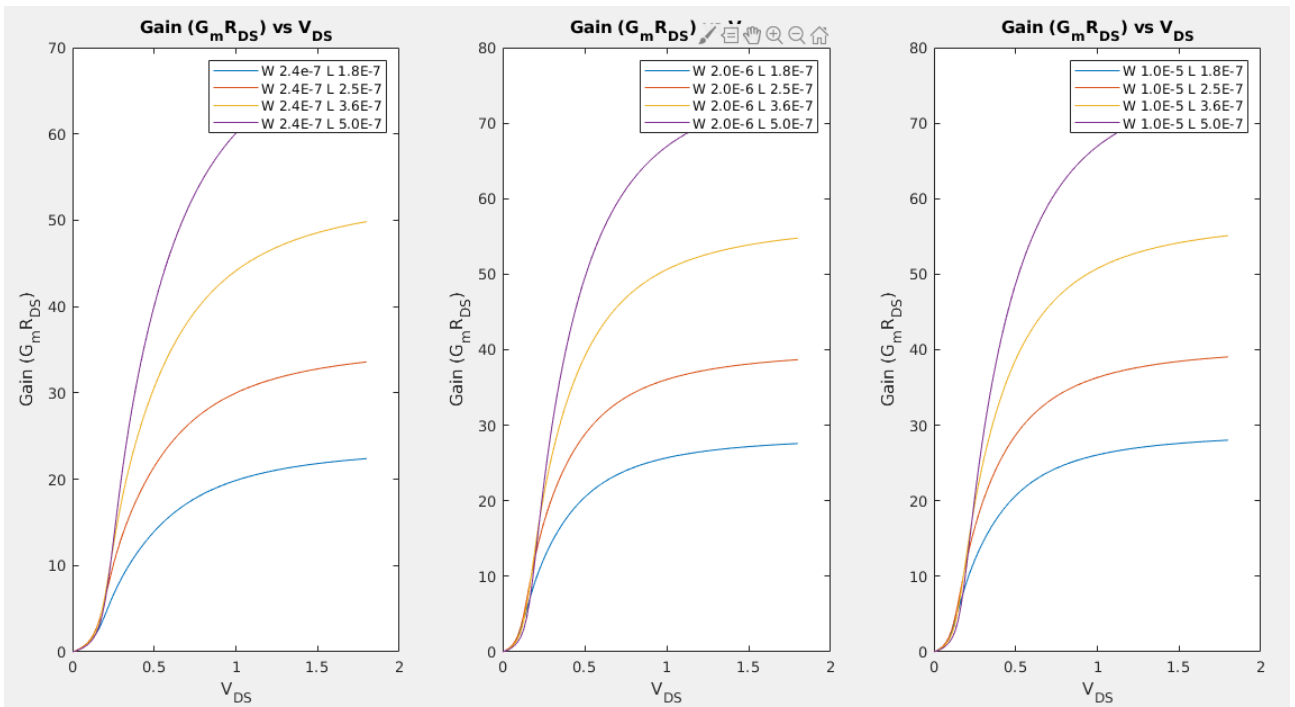


Figure 3: Plot of NMOS Gain vs V_{DS}

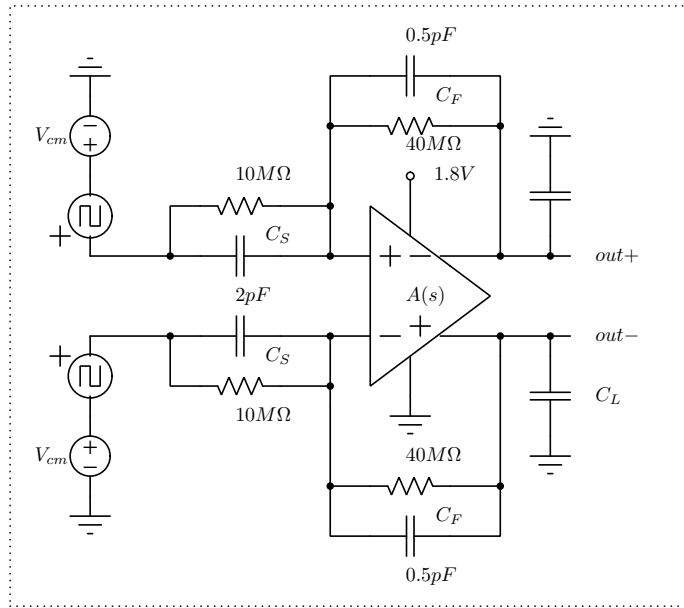


Figure 4: Amplifier in closed loop configuration

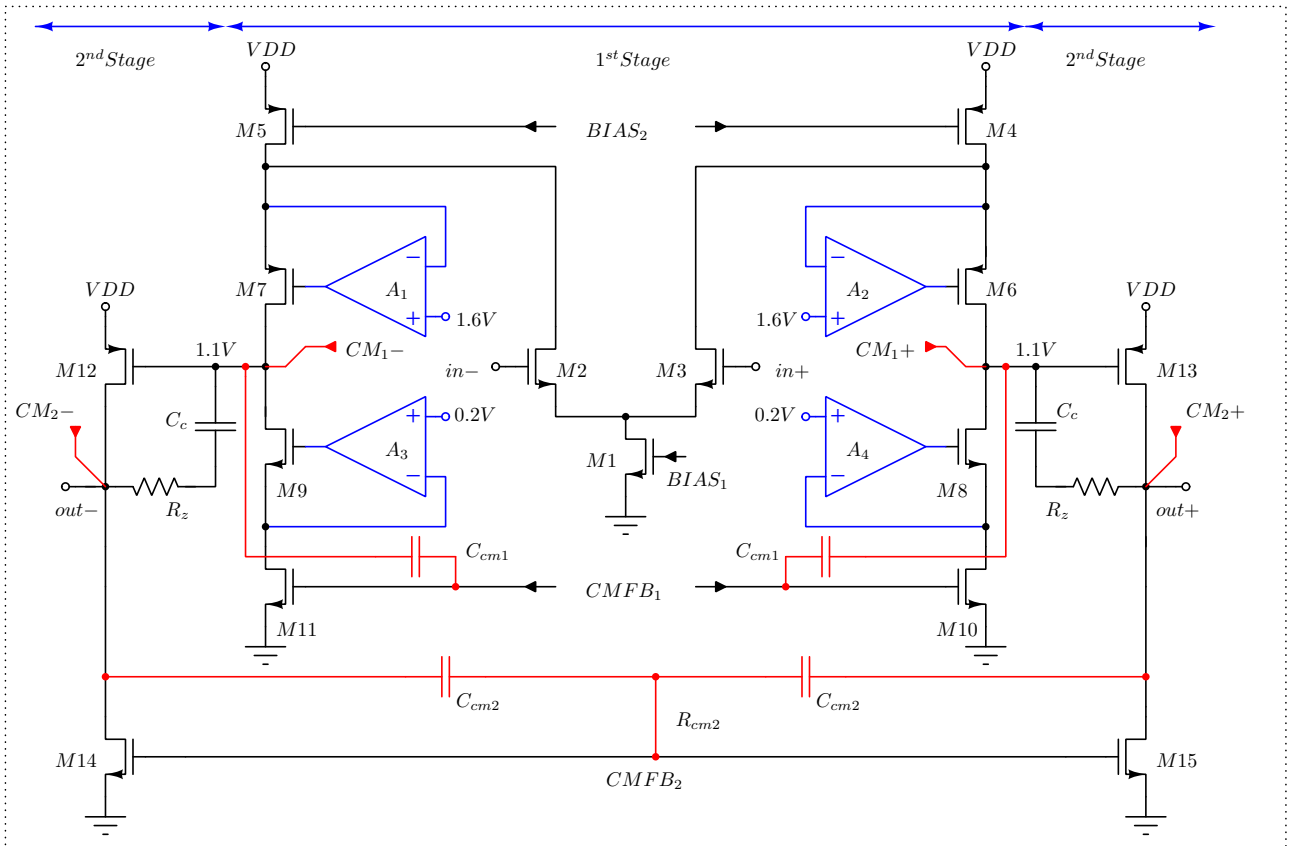


Figure 5: Two-stage Folded Cascode (Gain boosted) main amplifier; $C_c = 0.897pF$, $R_z = 950\Omega$; Components shown in "red" color are common mode feedback capacitors working with circuit mentioned in Fig. 8

Sr. No	Transistor Annotation	g_m	Current	Width	Length	Multiplier
1.	M1	22.11m	1.75m	6u	360n	40
2.	M2	18.18m	873.08u	28u	180n	20
3.	M5	23.31m	1.84m	60u	360n	20
4.	M7	12.45m	962.74u	8u	180n	20
5.	M9	10.90m	962.74u	2.5u	180n	20
6.	M11	11.17m	962.74u	6u	360n	20
7.	M12	25.23m	3.42m	10u	180n	80
8.	M14	22.45m	3.42m	6u	360n	80

Table 1: Parameters for Fig. 5

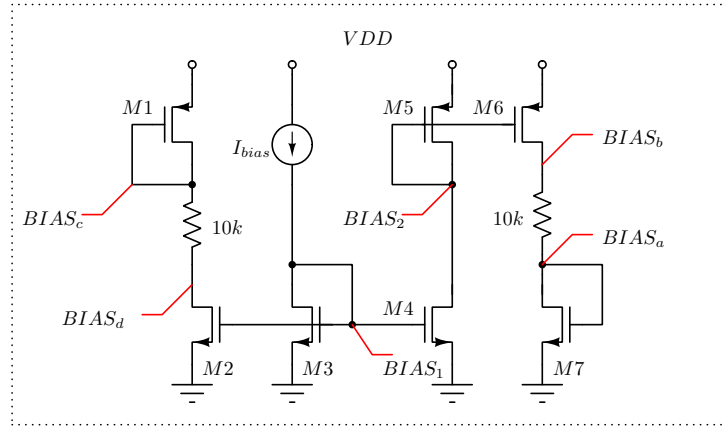


Figure 6: Principle Bias Network; $I_{bias} = 525 \mu A$

Sr. No	Transistor Annotation	Width	Length	Multiplier
1.	M1	22u	360n	1
2.	M2	2u	360n	1
3.	M3	4u	360n	20
4.	M4	4u	360n	20
5.	M5	21u	360n	20
6.	M6	22u	360n	1
7.	M7	2u	360n	1

Table 2: Parameters for Fig. 6

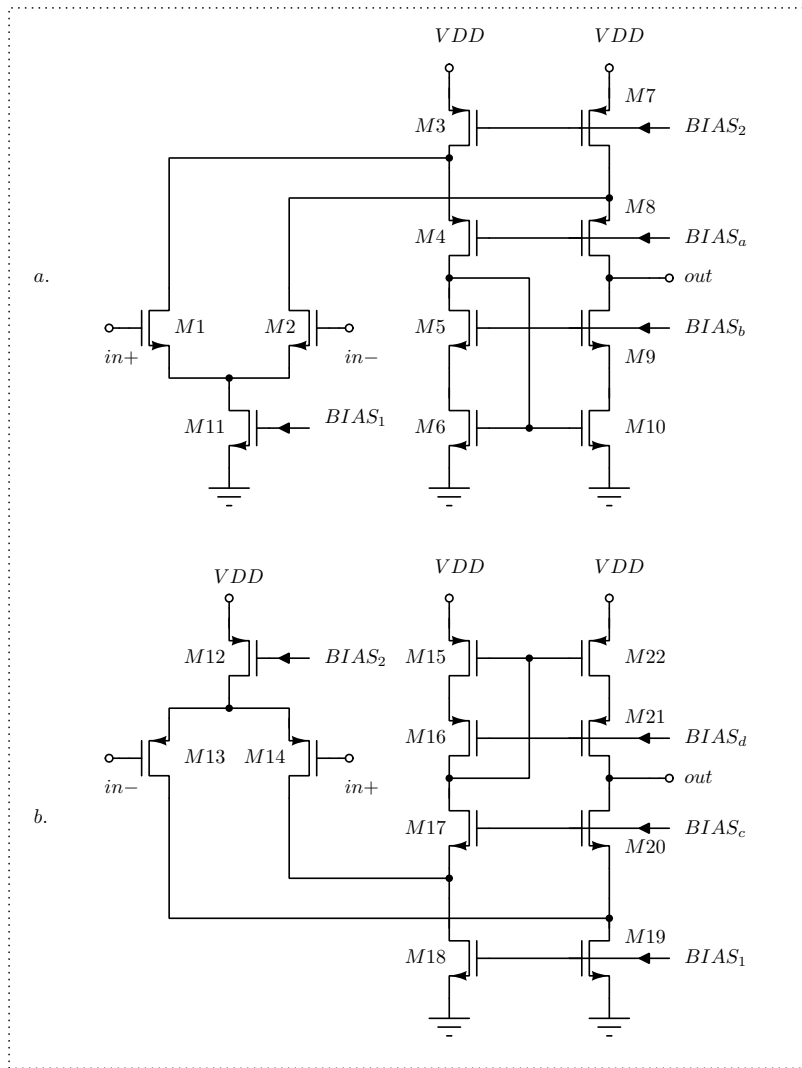


Figure 7: Gain Boosting Amplifiers; **a.** A_1, A_2 **b.** A_3, A_4 . Sizes have been kept 20 times less

Sr. No	Transistor Annotation	g_m	Current	Width	Length	Multiplier
1.	M1	137u	6.55u	5u	180n	1
2.	M2	134u	6.39u	5u	180n	1
3.	M11	294K Ω	12.95u	1u	360n	2
4.	M3	181K Ω	31.60u	22u	360n	2
5.	M4	376u	25.04u	8u	180u	1
6.	M5	345u	25.04u	2.5u	180n	1
7.	M6	108K Ω	25.04u	2u	360n	1
8.	M7	180K Ω	31.55u	22u	360n	1
9.	M8	368u	25.16u	8u	180n	1
10.	M9	358u	25.16u	2.5u	180n	1
11.	M10	111K Ω	25.16u	2u	180n	1
.						
1.	M13	55u	2.82u	10u	360n	1
2.	M14	68.82u	3.67u	10u	360n	1
3.	M12	1.33M Ω	6.49u	5u	360n	2
4.	M15	8.50K Ω	22.93u	22u	360n	2
5.	M16	349u	22.93u	8u	180u	1
6.	M17	338u	22.93u	2.5u	180n	1
7.	M18	129K Ω	25.04u	4u	360n	1
8.	M22	10K Ω	23.62u	22u	360n	1
9.	M21	365u	23.62u	8u	180n	1
10.	M20	329u	23.62u	2.5u	180n	1
11.	M19	128K Ω	26.44u	4u	360n	1

Table 3: Parameters for Fig. 7

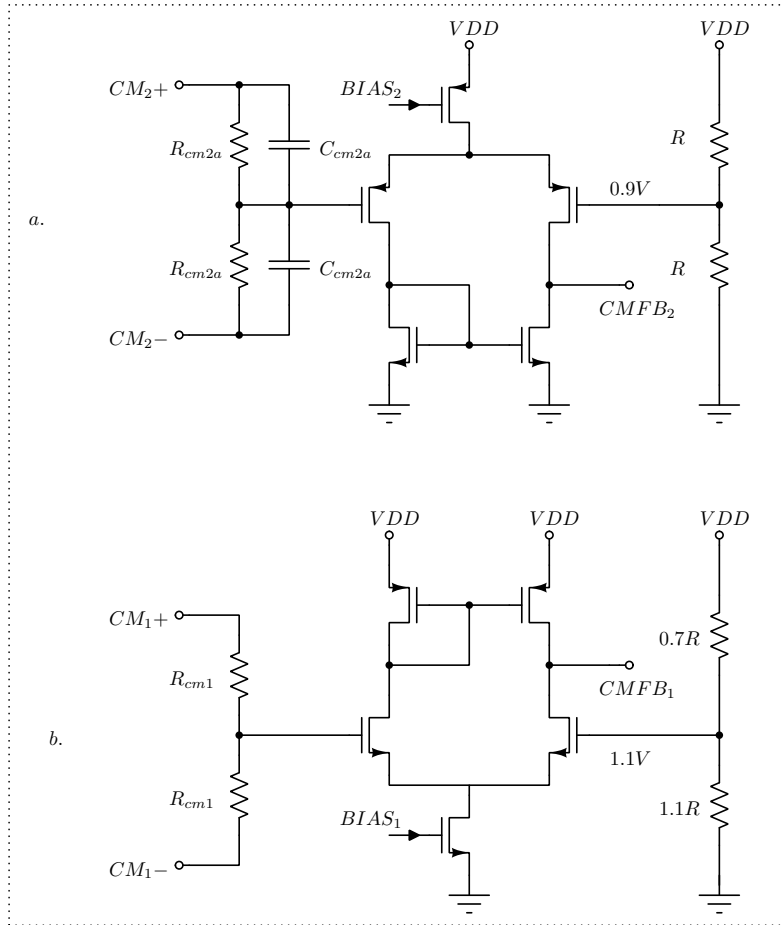


Figure 8: Common Mode Feedback Network; Some of CMFB capacitors are shown in Red color in Fig. 5

1.4 d

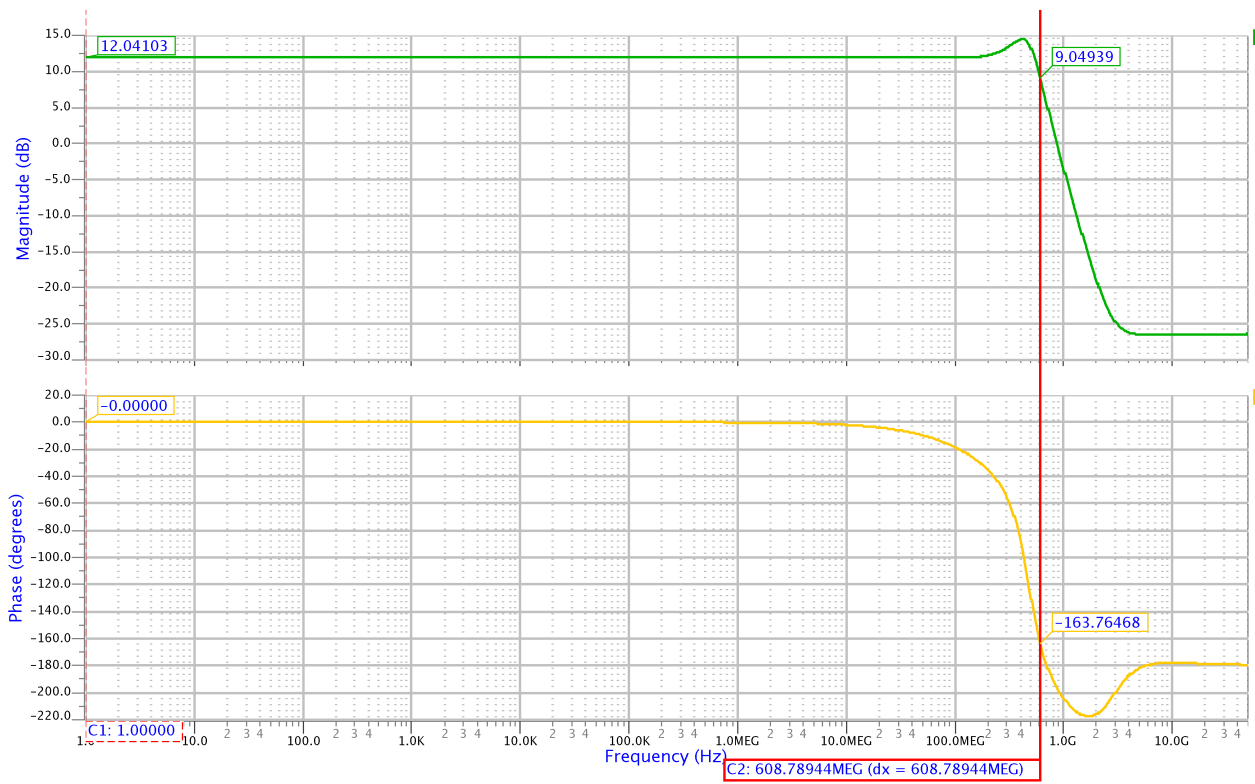


Figure 9: Closed loop Differential AC magnitude and Phase of $V_{out}(s)/V_{in}(s)$. DC Gain = 12.04 dB and -3dB Bandwidth = 608 MHz

1.5 e

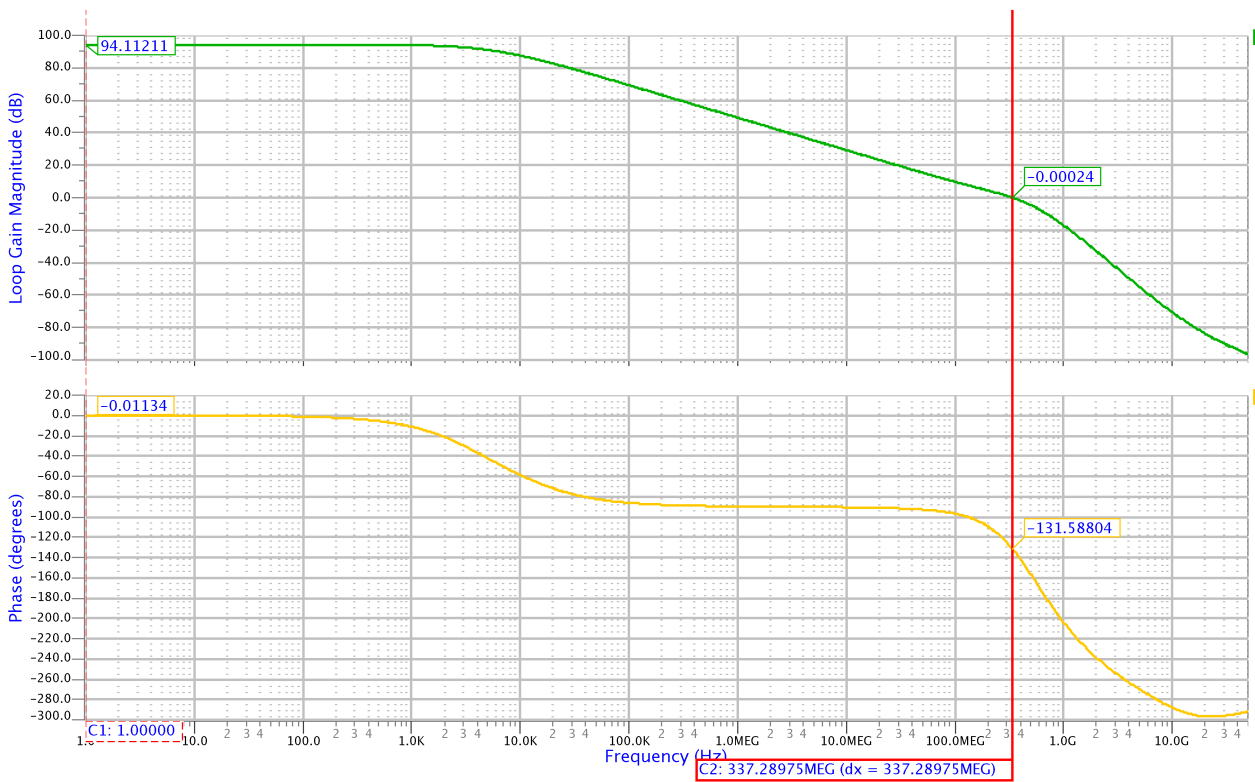


Figure 10: Differential Loop Gain (with β) Magnitude and Phase. DC Gain = 94.11 dB, UGB = 337.29 MHz, Phase Margin = 48.4°

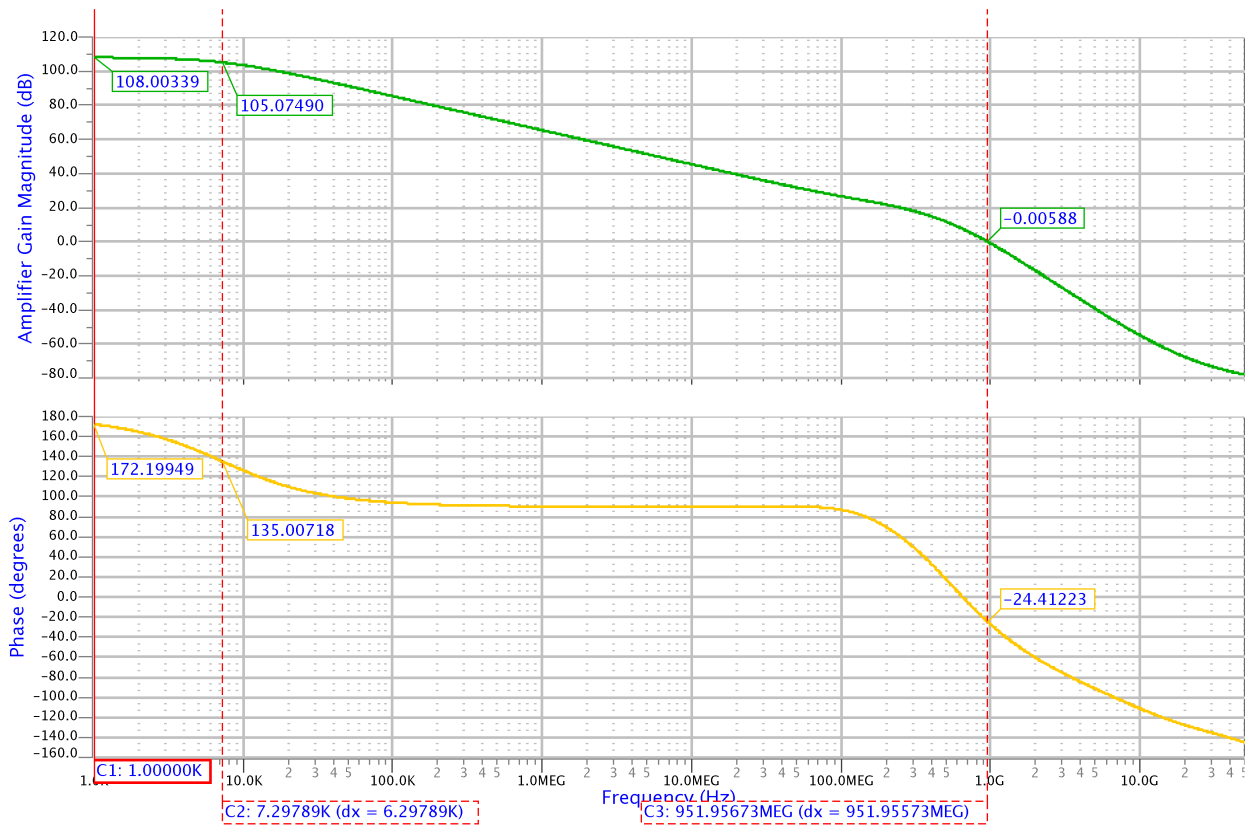


Figure 11: Open loop Amplifier (without β) differential Gain and Phase; Open loop amplifier is unstable while the closed loop amplifier is stable

1.6 f

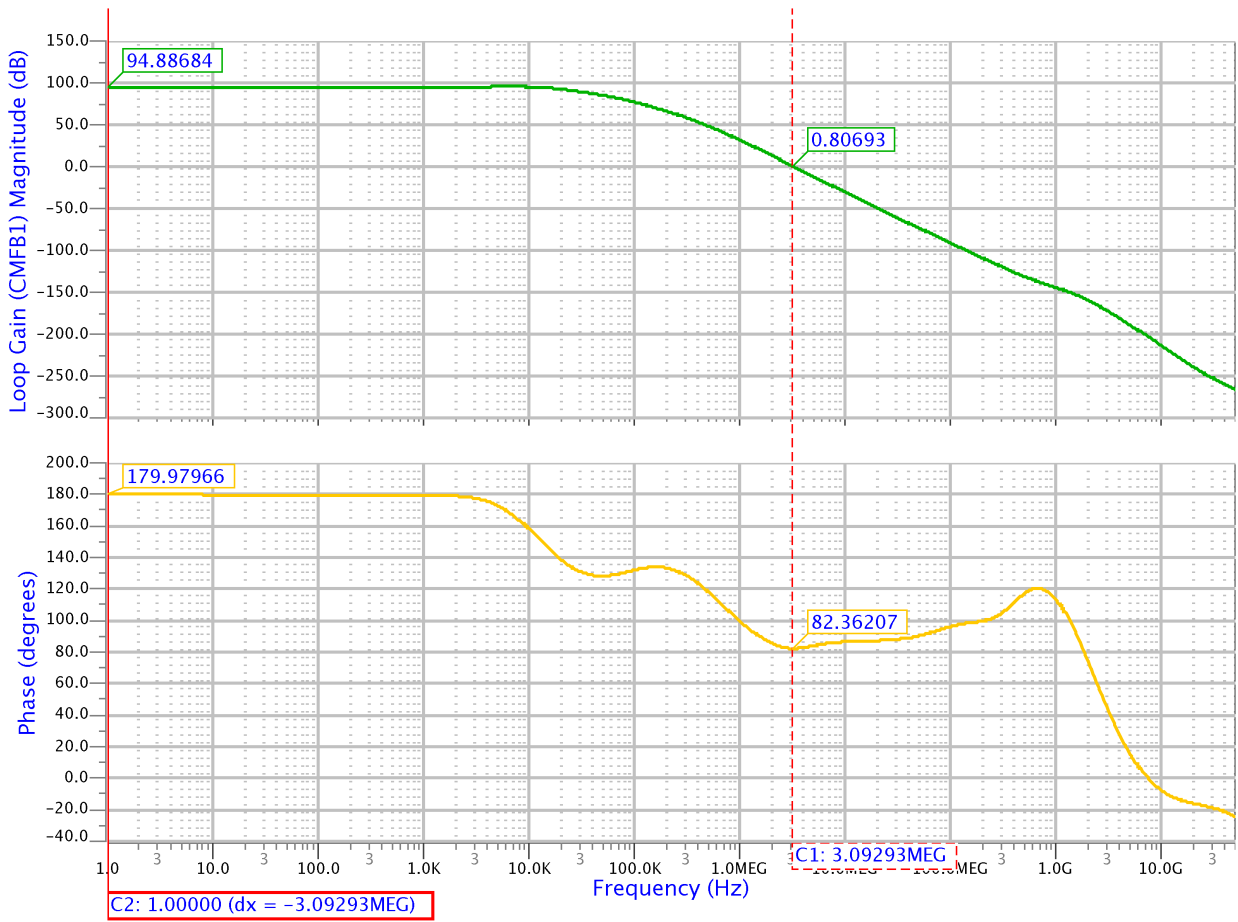


Figure 12: Differential Common-Mode Feedback (CMFB2) Loop Gain Magnitude and Phase. DC Gain = 94.88 dB, UGB = 3.09 MHz, Phase Margin = 82.36° (for circuit in Fig. 8.b)

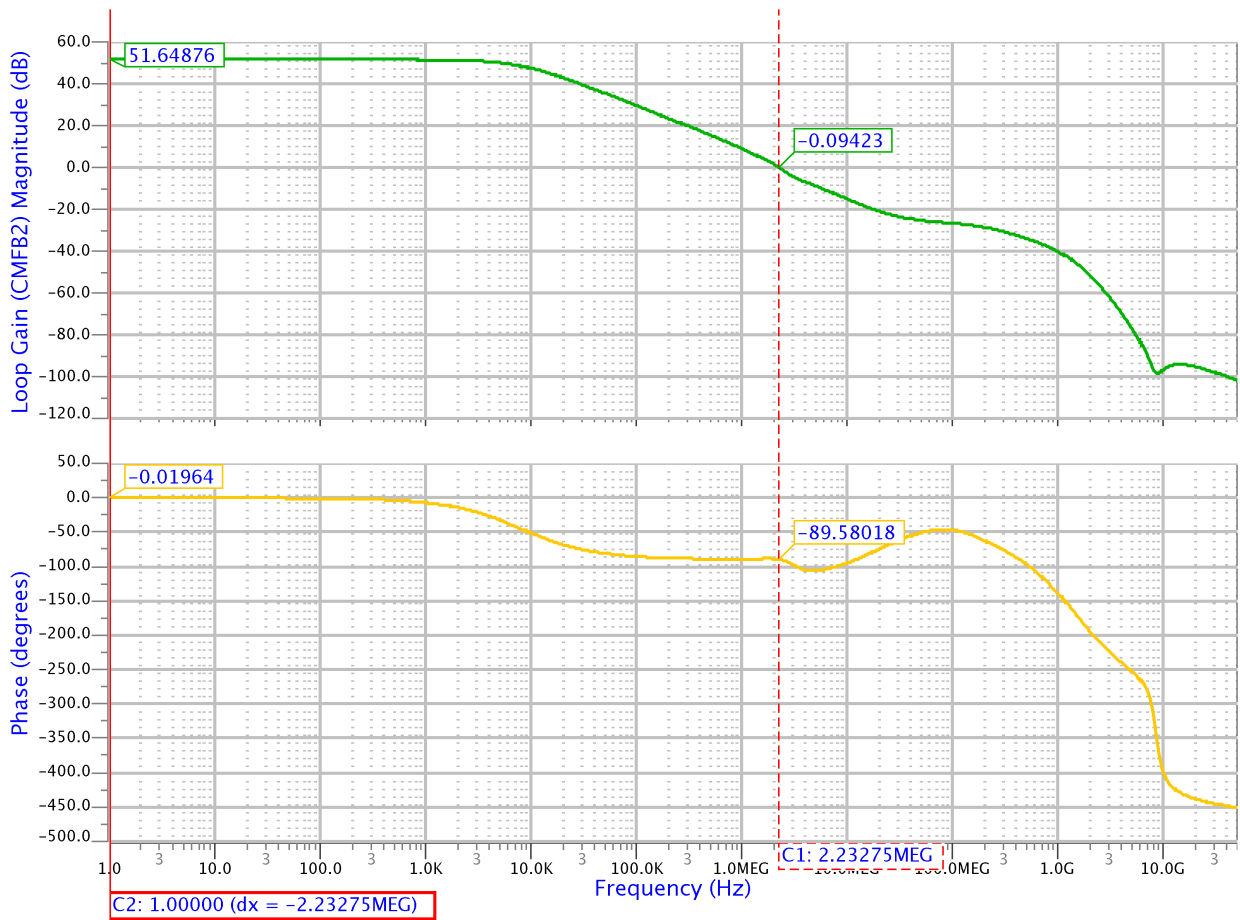


Figure 13: Differential Common-Mode Feedback (CMFB1) Loop Gain Magnitude and Phase. DC Gain = 51.65 dB, UGB = 2.233 MHz, Phase Margin = 90.42° (for circuit in Fig. 8.a)

1.7 g

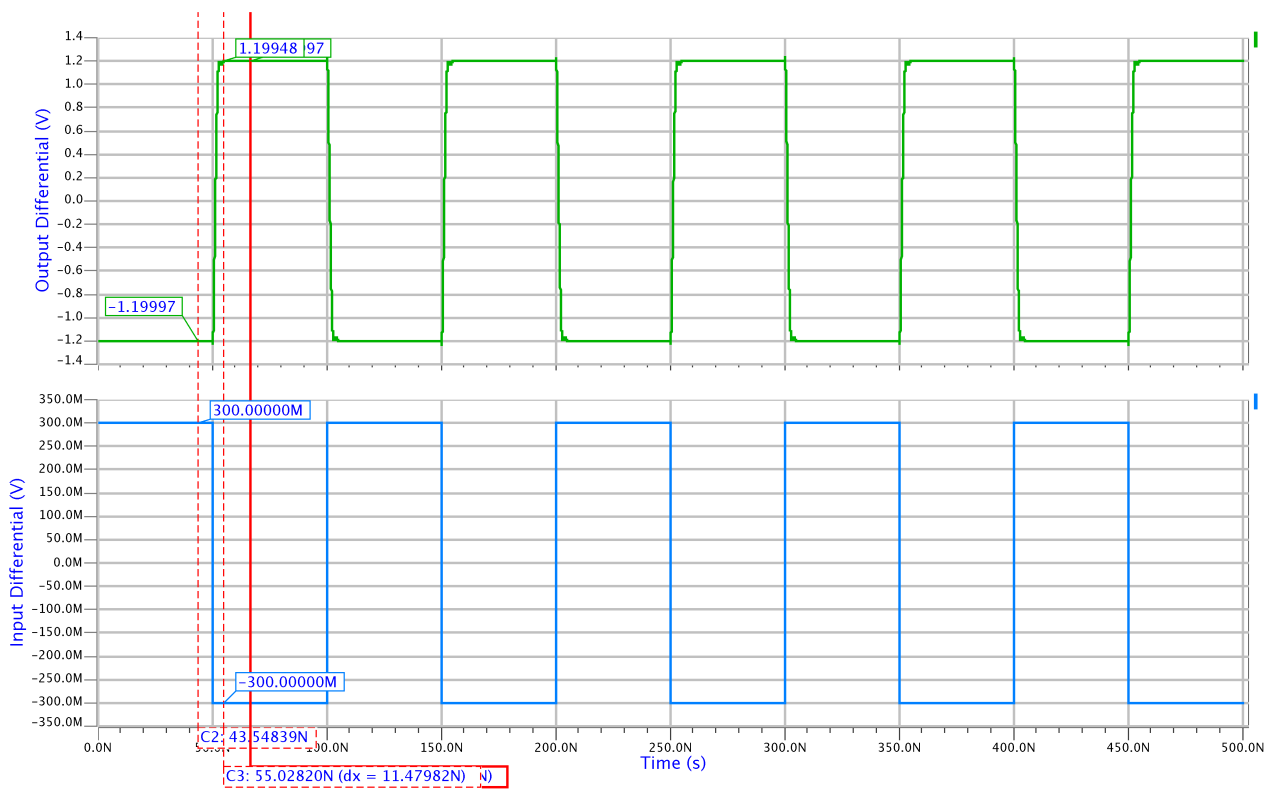


Figure 14: Differential Square wave transient response (to see if the common mode feedback is stable)

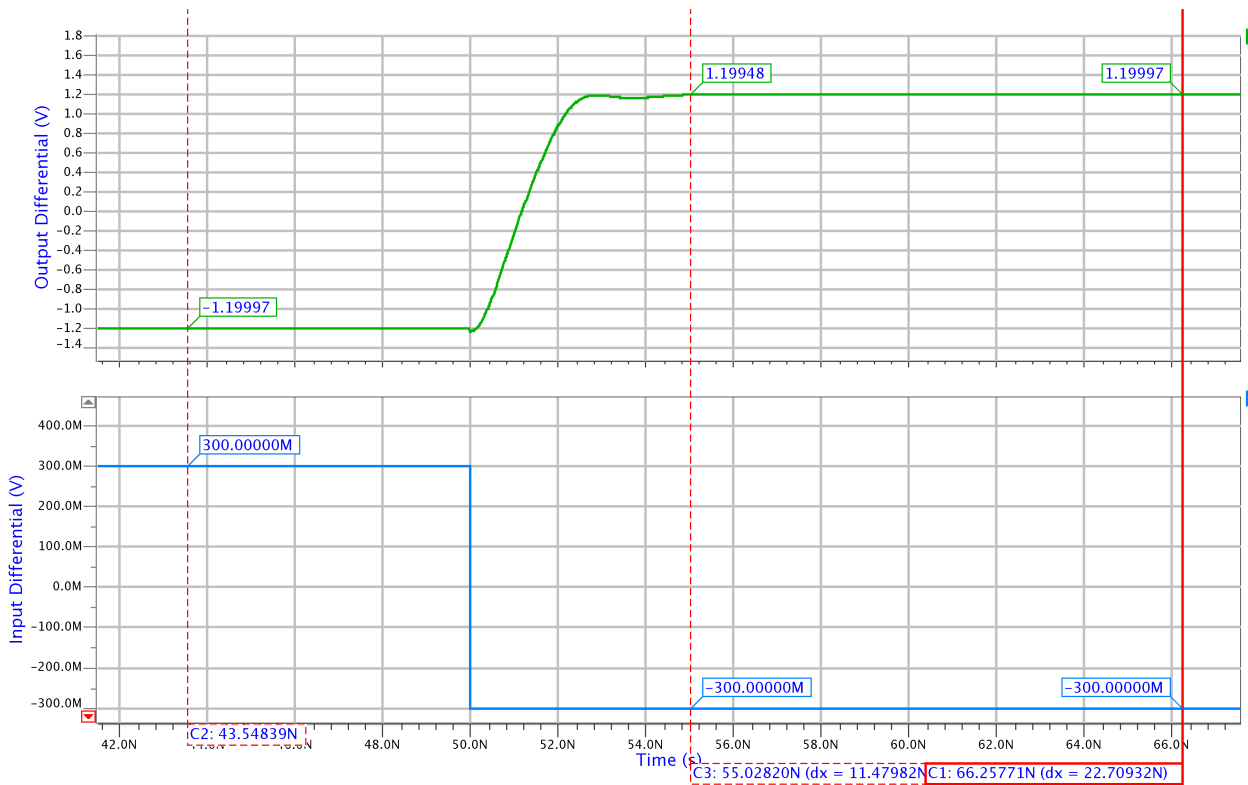


Figure 15: Differential Step Response (Output rise); Initial Output Voltage = -1.19997 V; Final Output Voltage = 1.19997 V; Settling error = 30 μV (0.0025 %); **Required specifications met.**

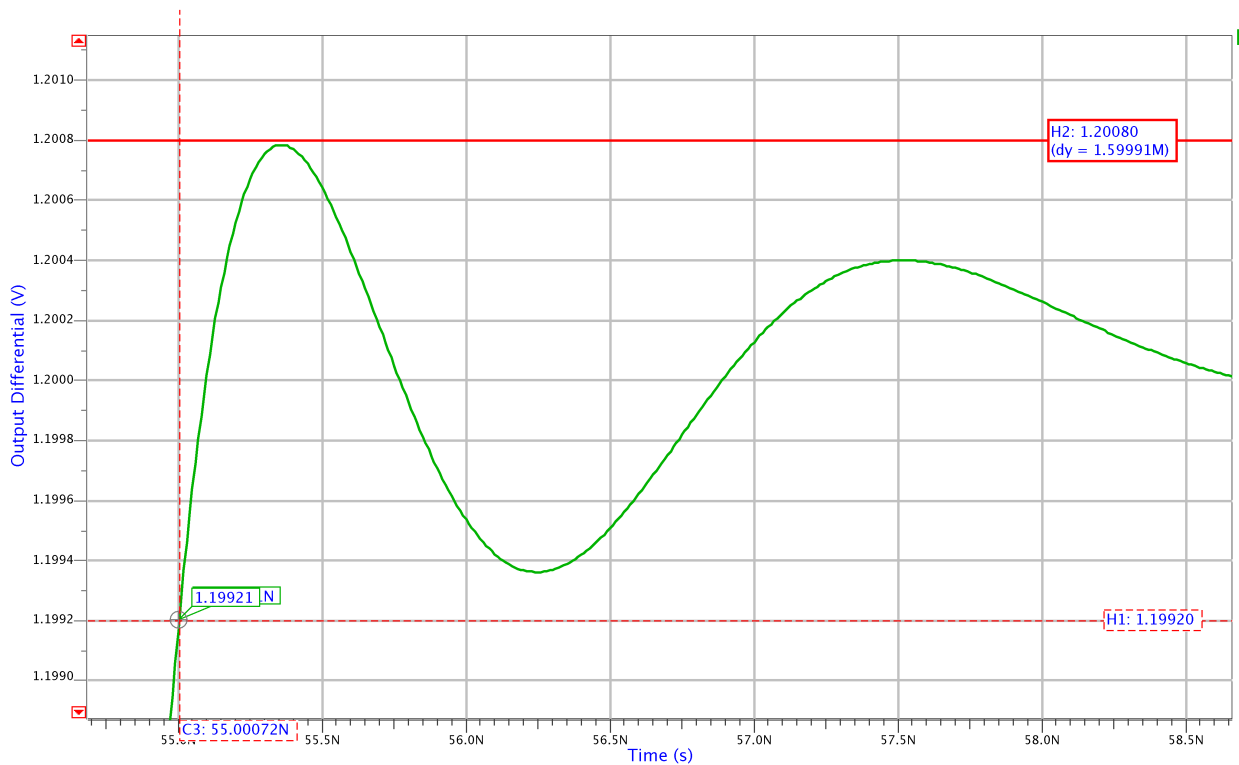


Figure 16: Enlarged Differential Step Response (Output rise); Settling time = 5 ns ($< 800 \mu V$); **Required specifications met.**

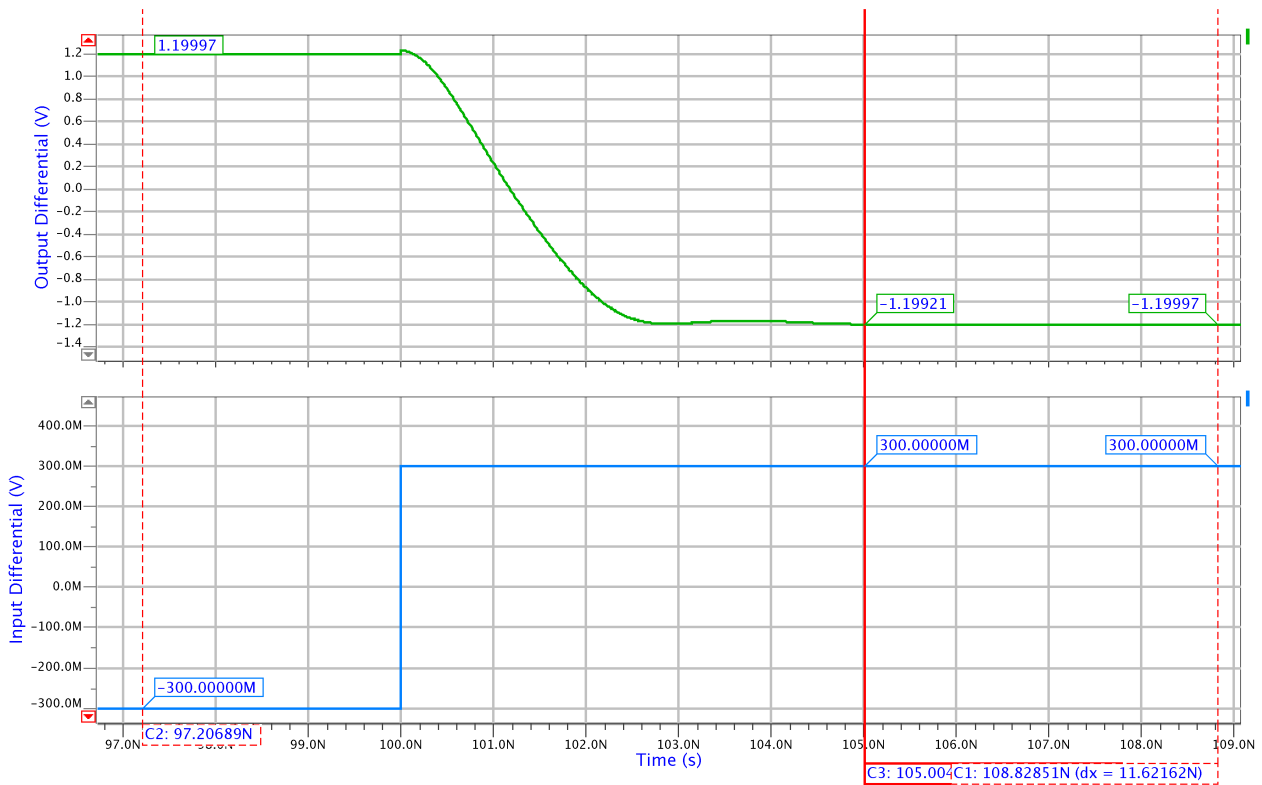


Figure 17: Differential Step Response (Output fall); Initial Output Voltage = 1.19997 V; Final Output Voltage = -1.19997 V; Settling error = 30 μ V (0.0025 %); **Required specifications met.**

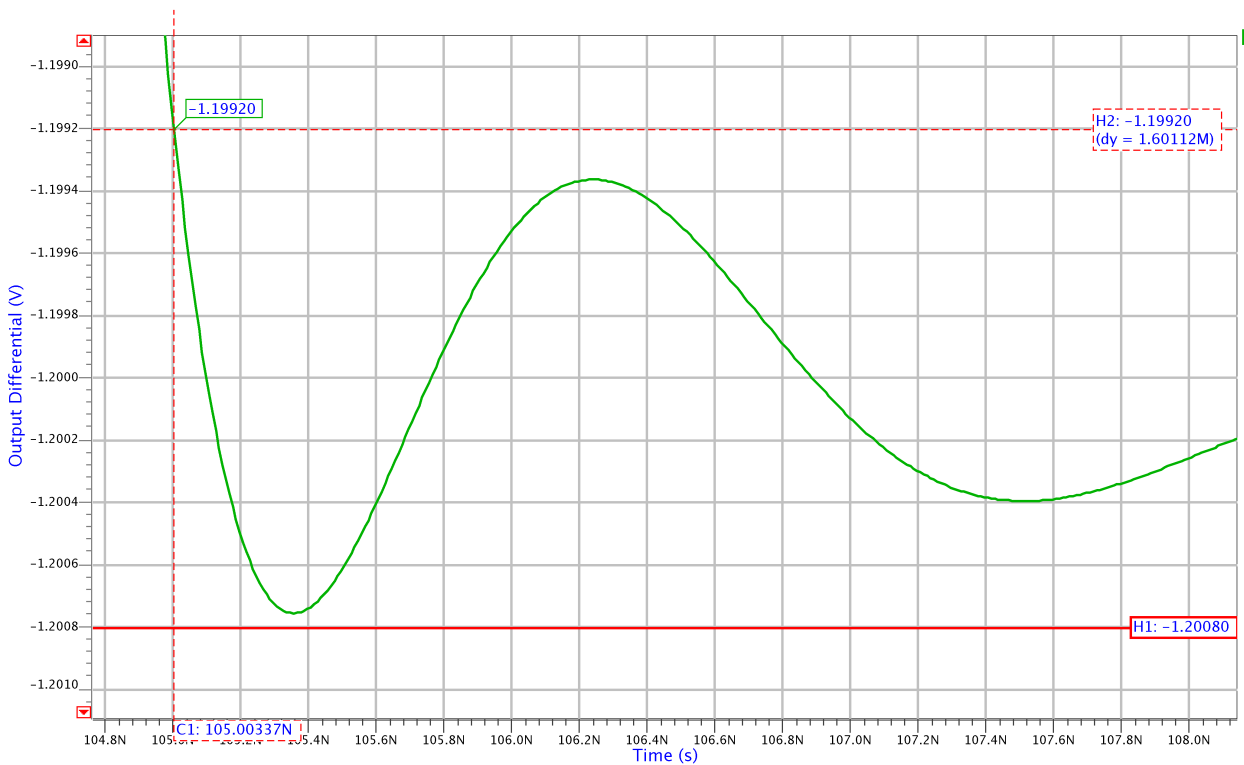


Figure 18: Enlarged Differential Step Response (Output fall); Settling time = 5 ns ($< 800 \mu$ V); **Required specifications met.**

2 Netlist

2.1 tb_tran_Amplifier_folded_cascode_rev1.cir

```
* Component: /home/ee18s063/Eldo_files/AIC_EE5320/Assignment_6/
tb_tran_Amplifier_folded_cascode_rev1 Viewpoint: default

.OPTION COMPAT
.INCLUDE "/home/ee18s063/Eldo_files/AIC_EE5320/Assignment_6/
tb_tran_Amplifier_folded_cascode_rev1/default/netlist.spi"
.OPTION AEX
.OPTION ENGNOT
.OPTION LIMPROBE=10000.0
.OPTION NOASCII
.DEFWAVE VDIFF_OUT = V(OUTP,OUTN)
.PLOT TRAN W(VDIFF_OUT)
.DEFWAVE VDIFF_IN = V(INN,INP)
.PLOT TRAN W(VDIFF_IN)

* - Analysis Setup - DCOP
.OPTION PROBEOP2
.OP

* - Analysis Setup - DC
.DC

* - Analysis Setup - AC
.AC DEC 1000 1 50G

* - Analysis Setup - LSTB
.LSTB X_AMPLIFIER_FOLDED_CASCADE_REV11.V4
.PROBE AC LSTB_P
.PROBE AC LSTB_DB

* — Global Outputs
.PROBE V SG

* — Params
.TEMP 27.0
.PARAM Ibias=0.525m
.PARAM Vpulse=0
.PARAM Rz=950
.PARAM Cc=0.897p
.PARAM Ccm=2.5p

* — Libsetup
.LIB KEY=TT "/home/ee18s063/Eldo_files/Models_UMC180/MM180_REG18-V124.lib" TT
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2.2 netlist.spi

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* ELDO netlist generated with ICnet by 'ee18s063' on Tue Apr 30 2019 at 20:52:59

.CONNECT GROUND 0

*
* Globals.
*
.global GROUND

*
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* Component pathname : /home/ee18s063/Eldo_files/AIC_EE5320/Assignment_6/
Amplifier_folded_cascode_rev1

*

.subckt AMPLIFIER_FOLDED_CASCODE_REV1 GNDA OUTN OUTP IXN IXP VDDA VOCM

M109 N\$1295 N\$1293 GNDA GNDA N_18_MM L=360n W=2u M=1
M108 VNP BIAS_B N\$1296 GNDA N_18_MM L=180n W=2.5u M=1
M107 N\$1293 BIAS_B N\$1295 GNDA N_18_MM L=180n W=2.5u M=1
M106 N\$1293 BIAS_A N\$1280 VDDA P_18_MM L=180n W=8u M=1
M105 VNP BIAS_A N\$1284 VDDA P_18_MM L=180n W=8u M=1
M102 N\$1282 BIAS1 GNDA GROUND N_18_MM L=360n W=1u M=2
M101 N\$1284 VNPS N\$1282 GROUND N_18_MM L=180n W=5u M=1
M100 N\$1280 N\$1281 N\$1282 GROUND N_18_MM L=180n W=5u M=1
R8 BIAS_B BIAS_A 10k NOISE=1
M99 BIAS_A BIAS_A GNDA GNDA N_18_MM L=360n W=2u M=1
M94 N\$1270 BIAS_B N\$1272 GNDA N_18_MM L=180n W=2.5u M=1
M93 N\$1270 BIAS_A N\$1257 VDDA P_18_MM L=180n W=8u M=1
M92 VPP BIAS_A N\$1261 VDDA P_18_MM L=180n W=8u M=1
M91 N\$1257 BIAS4 VDDA VDDA P_18_MM L=360n W=22u M=1
R5 OUTN_B N\$1339 Rz NOISE=1
R3 OUTP_B N\$1338 Rz NOISE=1
C3 N\$1338 OUTP Cc
R2 CM OUTP 10G NOISE=1
R1 OUTN CM 10G NOISE=1
M4 OUTN CMFB GNDA GNDA N_18_MM L=360n W=6u M=80
M3 OUTP CMFB GNDA GNDA N_18_MM L=360n W=6u M=80
M2 OUTN OUTN_B VDDA VDDA P_18_MM L=180n W=10u M=80
M1 OUTP OUTP_B VDDA VDDA P_18_MM L=180n W=10u M=80
R9 BIAS_C BIAS_D 10k NOISE=1
M134 BIAS_D BIAS1 GNDA GNDA N_18_MM L=360n W=2u M=1
M133 BIAS_C BIAS_C VDDA VDDA P_18_MM L=360n W=22u M=1
V13 N\$1326 GROUND DC 200m
M132 N\$1323 VNNS N\$1327 VDDA P_18_MM L=360n W=10u M=1
M131 N\$1327 BIAS4 VDDA VDDA P_18_MM L=360n W=5u M=1
M130 N\$1322 N\$1326 N\$1327 VDDA P_18_MM L=360n W=10u M=1
M129 N\$1323 BIAS1 GNDA GNDA N_18_MM L=360n W=4u M=1
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M126 N\$1316 BIAS_C N\$1322 GNDA N_18_MM L=180n W=2.5u M=1
M125 N\$1316 BIAS_D N\$1317 VDDA P_18_MM L=180n W=8u M=1
M124 VNN BIAS_D N\$1315 VDDA P_18_MM L=180n W=8u M=1
M35 VNNS CMFB1 GNDA GNDA N_18_MM L=360n W=6u M=20
M34 VPNS CMFB1 GNDA GNDA N_18_MM L=360n W=6u M=20
M33 OUTP_B VNN VNNS GNDA N_18_MM L=180n W=2.5u M=20
M32 OUTN_B VPN VPNS GNDA N_18_MM L=180n W=2.5u M=20
M31 OUTN_B VPP VPPS VDDA P_18_MM L=180n W=8u M=20
M123 N\$1317 N\$1316 VDDA VDDA P_18_MM L=360n W=22u M=1
M122 N\$1315 N\$1316 VDDA VDDA P_18_MM L=360n W=22u M=1
V11 N\$1309 GROUND DC 200m
M121 N\$1306 VPNS N\$1310 VDDA P_18_MM L=360n W=10u M=1
M29 VPPS BIAS4 VDDA VDDA P_18_MM L=360n W=60u M=20
M28 VNPS BIAS4 VDDA VDDA P_18_MM L=360n W=60u M=20
M116 VPN BIAS_C N\$1306 GNDA N_18_MM L=180n W=2.5u M=1
M115 N\$1299 BIAS_C N\$1305 GNDA N_18_MM L=180n W=2.5u M=1
M114 N\$1299 BIAS_D N\$1300 VDDA P_18_MM L=180n W=8u M=1
M113 VPN BIAS_D N\$1298 VDDA P_18_MM L=180n W=8u M=1
M112 N\$1300 N\$1299 VDDA VDDA P_18_MM L=360n W=22u M=1
M111 N\$1298 N\$1299 VDDA VDDA P_18_MM L=360n W=22u M=1
V10 N\$1281 GNDA DC 1.6
M110 N\$1296 N\$1293 GNDA GNDA N_18_MM L=360n W=2u M=1
M7 N\$1344 BIAS1 GNDA GROUND N_18_MM L=360n W=3u M=2

```

M6 N$1346 CMIN1 N$1344 GROUND N_18_MM L=360n W=3u M=1
M5 CMFB1 N$1343 N$1344 GROUND N_18_MM L=360n W=3u M=1
R6 OUTP_B CM1 10G NOISE=1
R4 CM1 OUTN_B 10G NOISE=1
M104 N$1280 BIAS4 VDDA VDDA P_18_MM L=360n W=22u M=1
M103 N$1284 BIAS4 VDDA VDDA P_18_MM L=360n W=22u M=1
C4 N$1339 OUTN Cc
M27 N$1227 BIAS1 GNDA GROUND N_18_MM L=360n W=6u M=40
M26 VNPS IXP N$1227 GROUND N_18_MM L=180n W=28u M=20
M22 VPPS IXN N$1227 GROUND N_18_MM L=180n W=28u M=20
M98 BIAS_B BIAS4 VDDA VDDA P_18_MM L=360n W=22u M=1
V9 N$1258 GNDA DC 1.6
M97 N$1273 N$1270 GNDA GNDA N_18_MM L=360n W=2u M=1
M96 N$1272 N$1270 GNDA GNDA N_18_MM L=360n W=2u M=1
M95 VPP BIAS_B N$1273 GNDA N_18_MM L=180n W=2.5u M=1
M90 N$1261 BIAS4 VDDA VDDA P_18_MM L=360n W=22u M=1
M89 N$1259 BIAS1 GNDA GROUND N_18_MM L=360n W=1u M=2
M45 N$1261 VPPS N$1259 GROUND N_18_MM L=180n W=5u M=1
M44 N$1257 N$1258 N$1259 GROUND N_18_MM L=180n W=5u M=1
M43 N$1254 N$1254 GNDA GNDA N_18_MM L=360n W=3u M=1
M42 CMFB N$1254 GNDA GNDA N_18_MM L=360n W=3u M=1
M41 N$1254 N$1255 N$1252 VDDA P_18_MM L=360n W=4u M=1
M40 N$1252 BIAS4 VDDA VDDA P_18_MM L=360n W=15u M=1
M39 CMFB VOCM N$1252 VDDA P_18_MM L=360n W=4u M=1
M38 BIAS4 BIAS4 VDDA VDDA P_18_MM L=360n W=21u M=20
M37 BIAS4 BIAS1 GNDA GNDA N_18_MM L=360n W=4u M=20
M36 BIAS1 BIAS1 GNDA GNDA N_18_MM L=360n W=4u M=20
I2 VDDA BIAS1 DC Ibias
M30 OUTP_B VNP VNPS VDDA P_18_MM L=180n W=8u M=20
M119 N$1305 N$1309 N$1310 VDDA P_18_MM L=360n W=10u M=1
M118 N$1306 BIAS1 GNDA GNDA N_18_MM L=360n W=4u M=1
M117 N$1305 BIAS1 GNDA GNDA N_18_MM L=360n W=4u M=1
C10 CMFB1 OUTP_B 250 f
C9 CMFB1 OUTN_B 250 f
M120 N$1310 BIAS4 VDDA VDDA P_18_MM L=360n W=5u M=1
C8 OUTN CMFB Ccm
C7 CMFB OUTP Ccm
C6 OUTP CM 250 f
C5 OUTN CM 250 f
R13 VOCM GNDA 10Meg NOISE=1
R7 VDDA VOCM 10Meg NOISE=1
V4 N$1255 CM 0
V1 CMIN1 CM1 0
V2 N$1343 GNDA DC 1.1
M9 N$1346 N$1346 VDDA VDDA P_18_MM L=360n W=4u M=1
M8 CMFB1 N$1346 VDDA VDDA P_18_MM L=360n W=4u M=1
.ends AMPLIFIER_FOLDED_CASCODE_REV1

```

```

*
* MAIN CELL: Component pathname : /home/ee18s063/Eldo_files/AIC_EE5320/
Assignment_6/tb_tran-Amplifier-folded-cascode-rev1
*

```

```

V7 N$60 IXP 0
V6 N$58 IXN 0
C3 INP IXP 2p
R3 IXP INP 10Meg NOISE=1
V3 INP N$54 AC 1 0 PATTERN Vpulse {-1*Vpulse} 0 1p 1p 50n
01010101010101010101010101010101
R1 OUTP IXN 40Meg NOISE=1
V5 INN N$15 AC 1 180 PATTERN {-1*Vpulse} Vpulse 0 1p 1p 50n
01010101010101010101010101010101

```

```
V2 N$15 GROUND DC 0.9
X_AMPLIFIER_FOLDED_CASCADE_REV11 GROUND OUTN OUTP N$58 N$60 N$38
+ N$48 AMPLIFIER_FOLDED_CASCADE_REV1
R2 IXN INN 10Meg NOISE=1
C6 GROUND OUTN 2p
C5 OUTP GROUND 2p
C4 IXP OUTN 0.5p
V4 N$54 GROUND DC 0.9
C2 INN IXN 2p
C1 IXN OUTP 0.5p
V1 N$38 GROUND DC 1.8
R4 OUTN IXP 40Meg NOISE=1
*
.end
```

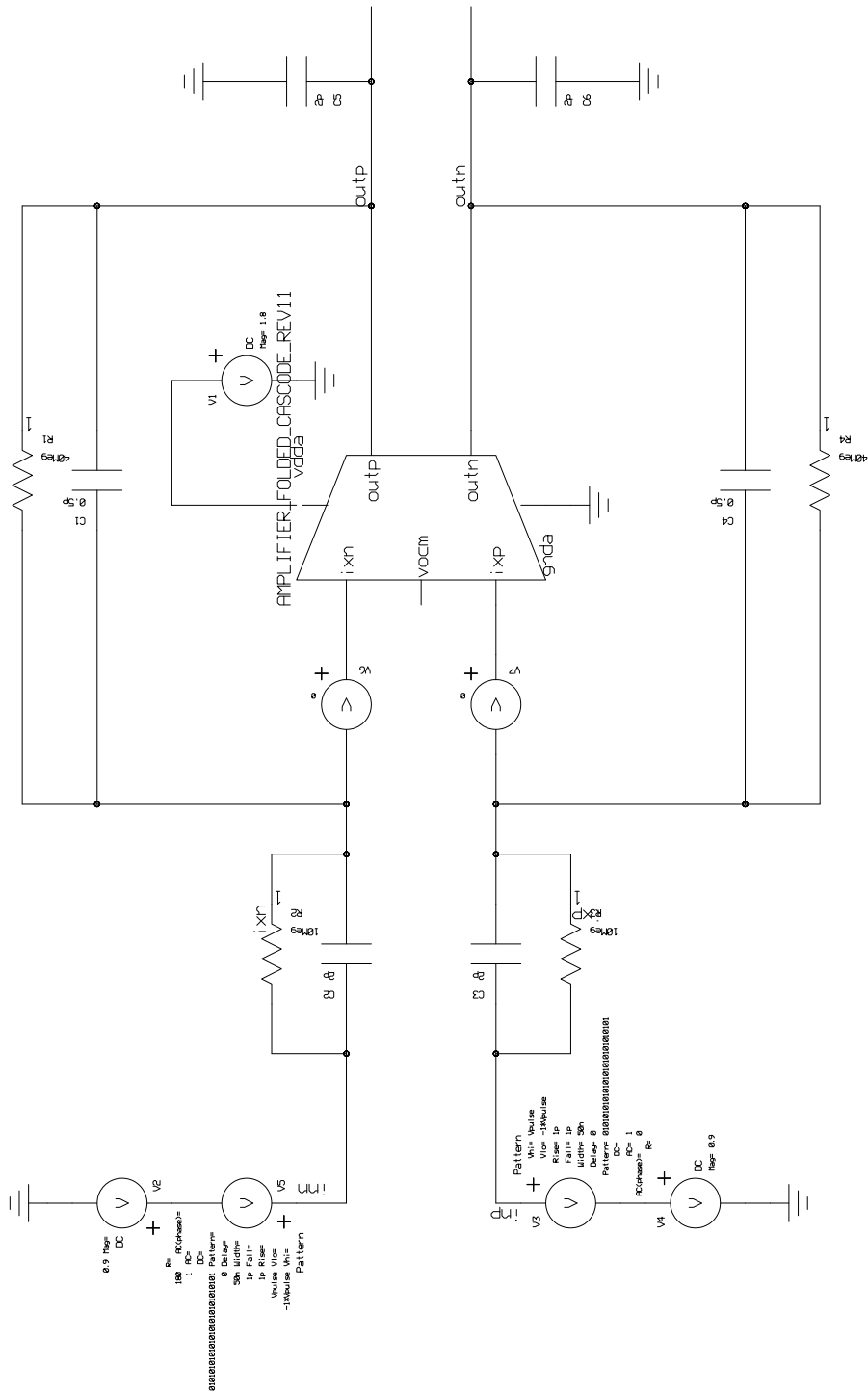


Figure 19: Pyxis Schematic of the Amplifier Test Bench

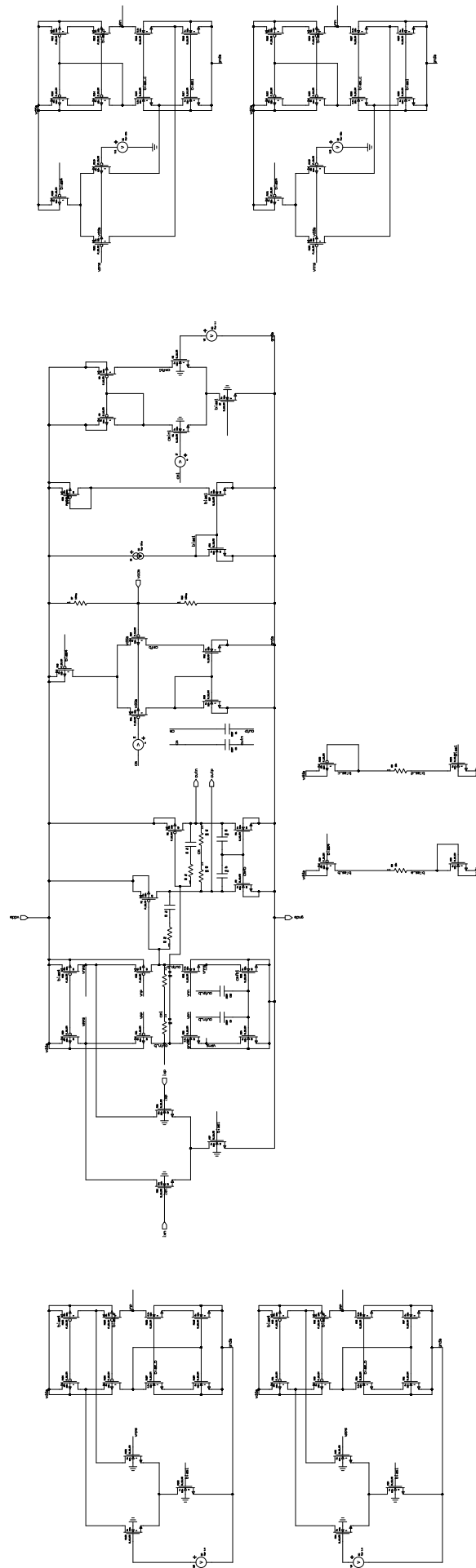


Figure 20: Pyxis Schematic of the Amplifier