A Project Report
on

COST OPTIMIZED ARBITRARY WAVEFORM GENERATOR USING DIRECT DIGITAL SYNTHESIS IN ARM CORTEX-M3/M4

Submitted in the Partial Fulfillment of the Requirements
for the award of

Bachelor of Technology
in
Electronics & Communication Engineering

By

Subha Sarkar
(20145120)
Tushar Kumar
(20145073)
Ashish Kumar Jha
(20145002)

Under the guidance of

Dr. Yogendra Kumar Prajapati
Assistant Professor

Department of Electronics & Communication Engineering
Motilal Nehru National Institute of Technology Allahabad
Allahabad - INDIA

(November , 2017)

UNDERTAKING

We declare that the work presented in this project titled **Cost optimized Arbitrary Waveform Generator using Direct Digital Synthesis in ARM Cortex-M3/M4** submitted to the DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING, MOTILAL NEHRU NATIONAL INSTITUTE OF TECHNOLOGY ALLAHABAD, ALLAHABAD for the award of the **Bachelor of Technology** degree in Electronics and & Communication Engineering is our original work. We have not plagiarized or submitted the same work for the award of any other degree. In case this undertaking is found incorrect, we accept that our degree may be unconditionally withdrawn.

March 27, 2019
Allahabad , INDIA

Subha Sarkar

Tushar Kumar

Ashish Kumar Jha

Department of Electronics & Communication Engineering
Motilal Nehru National Institute of Technology Allahabad
Allahabad - INDIA

CERTIFICATE

This is to certify that the work contained in the project titled **Cost optimized Arbitrary Waveform Generator using Direct Digital Synthesis in ARM Cortex-M3/M4**, submitted by **Subha Sarkar**, **Tushar Kumar** and **Ashish Kumar Jha** in the partial fulfillment of the requirement for the award of Bachelor of Technology in Electronics & Communication Engineering to the Electronics & Communication Engineering Department, Motilal Nehru National Institute of Technology, Allahabad, is a bonafide work of the students carried out under my supervision.

March 27, 2019
Allahabad , INDIA

(Yogendra Kumar Prajapati)
Assistant Professor
ECE Department
MNNIT Allahabad

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Allahabad , INDIA

Subha Sarkar

Tushar Kumar

Ashish Kumar Jha

ABSTRACT

The presented project is aimed at producing cost-effective arbitrary waveform generator by using the high-performance ARM®-Cortex-M3/M4 core of ARM® based Micro-Controller-Unit (MCU). The entire user application program and waveform generation program is designed to run on a single chip which reduces the cost considerably. Highly optimised assembly subroutine has been developed which not only maintains constant frequency resolution throughout the range of operation but also increases the sampling rate which is not achievable by a Non 32-bit MCU. The 32-bit General purpose registers are being used as phase accumulator, frequency & phase registers. Internal Static Random Access Memory (SRAM) is used to store the sampling data. The algorithm is implemented in assembly using THUMB instruction set.

A low-cost STM32F103 MCU from STMicroelectronics has been used to design the final product based on this project. This MCU has 16-bit General Purpose Input-Output (GPIO) port allowing a maximum of 16-bit vertical resolution. This project has been studied more on ARM®-architecture allowing the design to be manufacturer independent in terms of assembly subroutine. Using these MCUs, it is now possible to design very accurate, high precision, stable, compact (pocket-sized), power-efficient arbitrary waveform generator at highly afforable prices. It allows students to access more high-end test and measurement instruments.

The waveform is generated using Direct Digital Synthesis (DDS), which is a very common method to produce a digitally controlled, agile, temperature insensitive waveform. An on-board Rail-to-Rail power supply circuit has been designed to power the operational amplifiers. The output supports 50Ω load impedance driving capability for transmission line impedance matching.

The Universal Serial Bus (USB) 2.0 peripheral of the same MCU has been used to update firmware, download arbitrary waveform & control over USB from other USB complaint Host devices. The design supports sine wave frequency 0.01MHz - 1MHz (0.01Hz resolution), 10Vp-p (10-bit resolution).

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Chapter 1

INTRODUCTION

1.1 Introduction

The primary objective of this project is to provide a reasonable, cost-effective alternative to already present expensive arbitrary function/waveform generator. This would fill the gap present between a student in need and an expensive test & measurement instrument. Every electronics student/engineer needs at least a small but workable electronics workbench in his/her facility. It is always required to implement, test and debug the small ideas before proceeding forward in the design.

1.2 Motivation

A typical Direct Digital Synthesis [2] (DDS) waveform generator requires custom hardware (ICs) to sample and store the waveform samples. OEMs achieve this task by using either an ASIC or any programmable logic device like FPGA/CPLD. For storage either SDRAM or SRAM is used. These hardware are not only expensive but also require dedicated PCB designs (Multilayered, length matching, Isolation) requiring expensive manufacturing processes. Larger design require more hardware & software development cycles which increases cost.

A typical Micro-Controller-Unit (MCU) has a processing unit, volatile & Non-volatile memory which can mimic the FPGA/CPLD, SRAM/DRAM & EEPROM respectively. Although single cycle sampling is not possible as in ASIC & Programmable Logic Devices, it is possible using MCU in dozen of cycles. The choice of architecture plays a vital role in achieving higher sampling rates. In 8-bit or 16-bit MCUs, any 32-bit operation is segmented into multiple tasks by the compiler. This seriously decreases high integer operation rate. Most of 8-bit and 16-bit MCUs have been found to run at $\leq$ 16 MHz frequency. This further undermines the capability of such cores.

A very popular architecture called ARM provides uniform development platform across various silicon manufacturers. It outperforms 8051 and other contemporary architectures through its powerful 32-bit architecture, 3-stage pipeline, high core speed through integrated PLL, large

SRAM & Flash, higher peripherals, superior interrupt handling capability (Nested Vectored Interrupt Controller (NVIC)) and more.

1.3 Basic Concepts

Most of the waveforms in nature are non-linear e.g., sine wave. These type of waveforms are typically generated using either RC oscillators (Analog way) or piecewise contruction (Digital way & sometimes analog way). The phase information is linear in nature. It means that the phase angle rotates a fixed angle for each unit of time.

We know,

$$\omega = 2\pi f \tag{1.1}$$

$$\omega_{out} = 2\pi F_{out} \tag{1.2}$$

$$\Delta\theta = \omega\Delta t \tag{1.3}$$

ω is the angular frequency & F_{out} is desired frequency of the waveform. Now it is required to store the sample in an address which is a discrete value. The increase in address can be extracted from $\Delta\theta$. Δt signifies the change in time after one sampling interval, $T_{sampling}$. Let the sampling frequency is $F_{sampling}$,

Then,

$$\Delta t = \frac{1}{F_{sampling}} = T_{sampling} \tag{1.4}$$

$$F_{sampling} = \frac{F_{pll}}{N} \tag{1.5}$$

F_{pll} is the core clock speed decided from the configuration of PLL inside the MCU. N is the number of effective cycles elapsed to sample one value from the memory (SRAM). The value of N has been found to be 12 (Refer Algorithm & Implementation at pg. 11).

The phase ranges from $0-2\pi$. To represent it digitally we dedicate a register $R_{frequency}$ of n-bit. Although it stores phase information it is called $R_{frequency}$ because F_{out} depends directly on it. Now ,

$$\Delta\theta = \frac{2\pi}{2^n} \times R_{frequency} \tag{1.6}$$

It is clear from (1.6), to obtain highest phase resolution, higher value of n is preferred. So we choose 32-bit registers from ARM core. Inserting the value of $\Delta\theta$ from (1.6) & Δt from (1.5) to

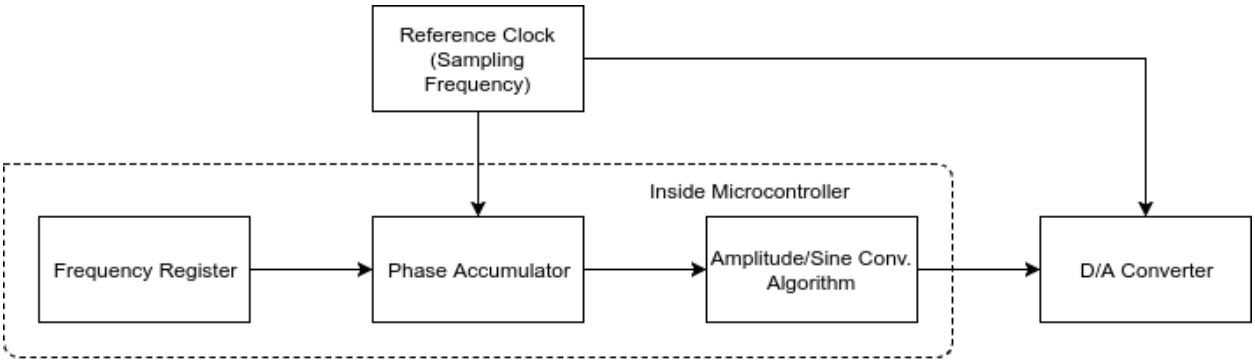


Figure 1.1: Block Diagram of the DDS scheme implemented in this project

(1.3), we obtain -

$$\frac{2\pi \times R_{frequency}}{2^n} = \frac{2\pi \times F_{out}}{F_{sampling}} \tag{1.7}$$

$$\frac{R_{frequency}}{2^n} = \frac{F_{out} \times N}{F_{pll}} \tag{1.8}$$

$$R_{frequency} = \frac{F_{out} \times N \times 2^n}{F_{pll}} \tag{1.9}$$

Using this formula the value of $R_{freqeuncy}$ is calculated for a desired value of F_{out}. The value is inserted to $R_{frequency}$ and added to R_{phase} on each $T_{sampling} = \frac{1}{F_{sampling}}$. Now each value of R_{phase} represents a unique phase corresponding to an address in SRAM. Since it is a 32-bit register, it can address 2^{32} unique locations that is approximately 4G of memory. It is impractical to use such huge amount of memory just to represent 10-bit sample values.

10-bit sample values can have maximum of 1024 unique values so, 10-bit addressable memory is sufficient. To reduce phase noise we use more copies of each sample. Phase noise occurs due to continous drift in phase after each overflow of the R_{phase}. In this design we have decided to use 4-copies, adding 2 more bits to the address. Hence we have 12-bit address of the samples. We require $2^{12} \times 10$ SRAM. Memory read/write operation in ARM Cortex M3 supports 3 alignments namely byte aligned (8-bit), half-word aligned (16-bit) & word aligned (32-bit). Half-word aligned memory is suitable for this application. The MSB 12-bits are extracted and added as offset with base address register. The resulting address provides the sample value.

[Base register + Register offset] addressing mode is used to fetch the data. The core is basically a load-store architecture so the data has to be stored first inside the General Purpose Registers. The data is fetched and stored back to the required General Purpose Input-Output (GPIO) register using [Register Addressing] mode.

1.4 Specifications and Design

Table 1.1 provide necessary specifications to be implemented.

Sr. No	Properties	Values
1.	Voltage Swing	10 Vpp
2.	DC Offset	2.5 V
3.	Resolution	10-bits
4.	Frequency (Sine)	1 MHz
5.	Frequency (Rectangle)	100 KHz
6.	Output Impedance	50 Ω
7.	Frequency Resolution	0.01Hz
8.	Power Supply (Positive Rail)	+8V
9.	Power Supply (Negative Rail)	-8V
10.	Power Supply (Ripple)	25 mVpp
11.	Power Source	USB
12.	Input Voltage Supply	+5 V
13.	Output Display	LCD 16X2 (HD44780)
14.	Miscellaneous Feature	Arbitrary Waveform

Table 1.1: Design specifications to be implemented

Chapter 2

EMBEDDED DESIGN

2.1 ARM® Cortex® M

ARM Cortex M is a modern processor architecture designed by Advanced RISC Machines (ARM) Ltd. for deep embedded applications requiring low gate counts, deterministic latency & low cost devices. Other architectures designed by ARM are Cortex A & R series which target Application & Real-time processing respectively. Only ARM Cortex M is discussed here.

2.1.1 Architectural overview

It is one of the ARMv7-M [9] Harvard family of processors from ARM®. It is an Harvard-Architecture [8] : having a separate instruction & data bus. This feature is important in piplined CPU where at the same time CPU could be accessing the data & instruction bus. Since it is a RISC architecture, it deploys load-store form of data manipulation. ARM® Cortex® M3 is the evolved version of ARMv4T (Von-Neumann) suiting MCU application. However it inherits a lot of benefits of application processor from its predecessor. It supports THUMB/THUMB-2 Instruction set. THUMB-2 allows mixed THUMB (16-bit, High code density, Less powerful) & ARM (32-bit, Poor code density, Powerful) instruction whenever required, which maintains the code desity as found in 8-bit & 16-bit MCU while retaining the performance of 32-bit MCU.

Advanced High-performance Bus (AHB) forms the backbone of data flow between the ARM core & other parts. It is connected to Advanced Peripheral Bus (APB) using APB Bridge as shown in Figure 2.2. APB allows dynamic shutdown of peripherals to save power. Internal Memory (SRAM, FLASH) & Direct Memory Access (DMA) Controller are directly connected to AHB while the Custom GPIO peripherals are connected with APB. This is due to the fact that high speed memory operations require dedicated short path to the core. Hardware multiplication is done in single cycle (32x32 bit). ARM® Cortex® M3 does not support direct floating point instructions like ARM® Cortex® M4. It is required to call separate subroutines to do the operations which is handled by the compiler. Hardware division is multiple cycle operation.

The interrupt architecture is also superior to some popular 8-bit MCU. It has a tighly coupled

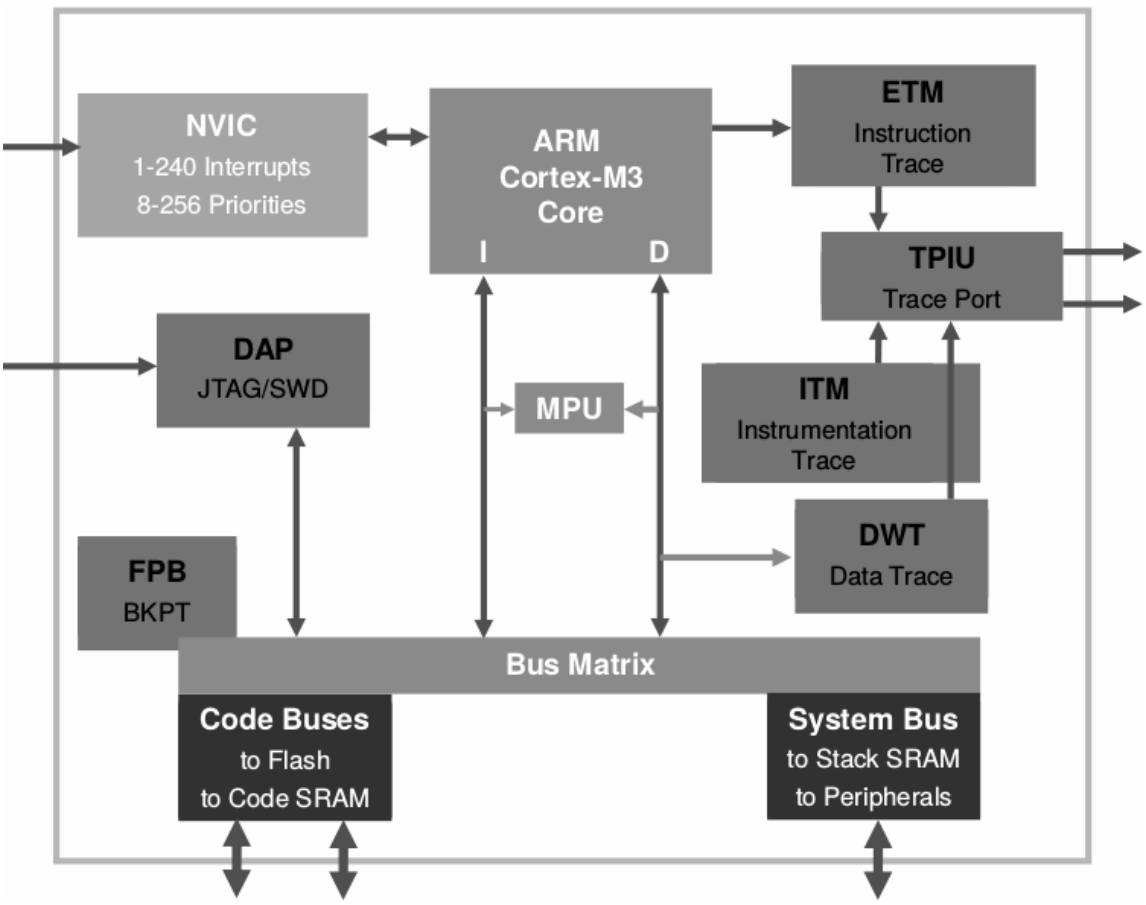


Figure 2.1: Block diagram representation of internal components of ARM Cortex M3 Processor (Source : ARM® Infocenter)

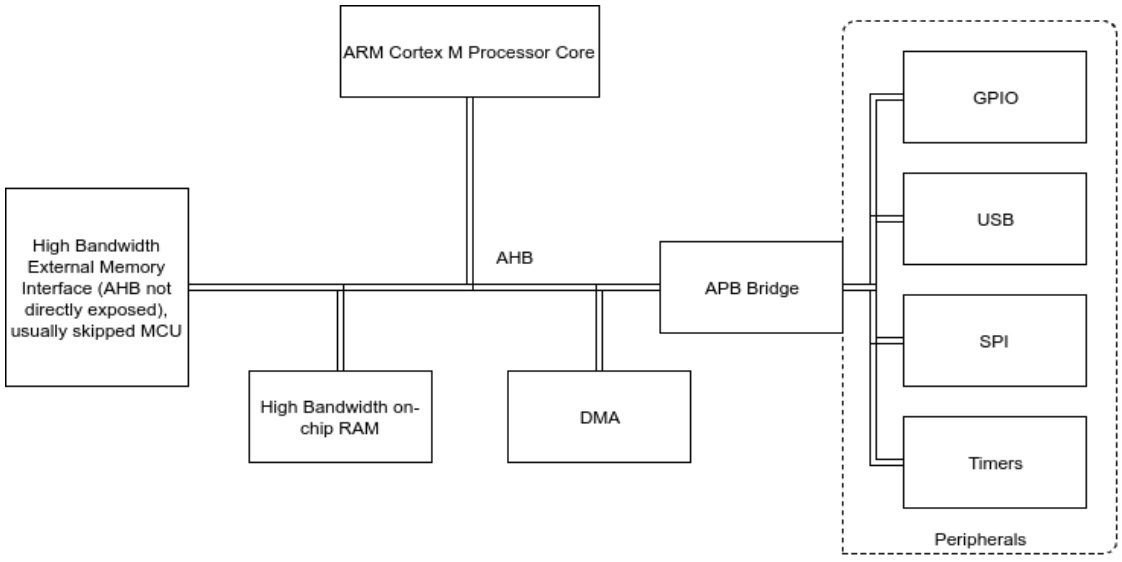


Figure 2.2: Advanced Microcontroller Bus Architecture (AMBA) system in ARM Cortex M3 based MCU (Source : ARM® Infocenter)

NVIC which not only allows 1-240 external interrupts but also dynamically changeable 255 levels of priorities of each interrupt. Every interrupt can be set as either level triggered (High & Low), or edge triggered (Positive & Negative edge)

2.1.2 3-Stage pipeline

The study of pipelined [3] stages of this architecture is very important as it allows us to justify the value of N & sometimes estimate it correctly. The pipeline is a method to achieve parallism in uni-processor system. A bigger task is divided into multiple tasks so that each tasks can be executed at the same time. The diagram of pipeline system of ARM® Cortex® M3 is shown in Figure 2.3. The 3-stages namely **Fetch**, **Decode**, **Execute** are common in most of the architectures. Interesting thing about the execute phase here is it does the write back also, which is found to be another stage in some 4-stage pipelined architecture. To achive single cycle operation it is required to first fill the pipeline stages. The assembly subroutine has 11-tasks (T, not to be confused with N) (assuming 2 cycles of operation for LDRH, STR, LDR). So here the pipeline efficiency decreases. For achieving higher pipeline efficieny it is required to have $T \to \infty$. This can be done by copying the assembly subroutine multiple times which effectively increases T. The problem is now the increased phase noise due to rippling sampling interval ($T_{sampling}$) or some sort of jitter. This is happening due to the last branch instruction which fluses the pipeline & varies the $T_{sampling}$. The effective $F_{sampling}$ saturates to $\frac{F_{pll}}{11}$ which is not too high. So increase in T effectively compromising the performance of the system. Pipeline efficiency is a very important parameter in parallism. It is given by-

$$\eta = \frac{T}{T+S-1} \times 100 \tag{2.1}$$

$$\eta = \frac{11}{11+3-1} \tag{2.2}$$

$$\eta = 84.61\% \tag{2.3}$$

Here η denotes efficiency in % & S denotes stages in pipeline. Closer is the value of η to 100% better the speed up ratio.

2.1.3 Peripheral & Memory organisation

The deepest level of control is achievable through assembly programming. For assembly programming it is must to know the instruction set architecture (ISA), memory organisation, and peripheral interfaces. Figure 2.4 shows the common memory map. It is now evident that it is not I/O mapped I/O but memory mapped I/O organisation. There are no separate instructions for I/O operations. Register addressing mode can be used to do the I/O operations.

During boot process the processor scans the external BOOT1 and BOOT0 pin for selecting the boot sector. BOOT0 has been pulled down to ground so that the internal flash memory is

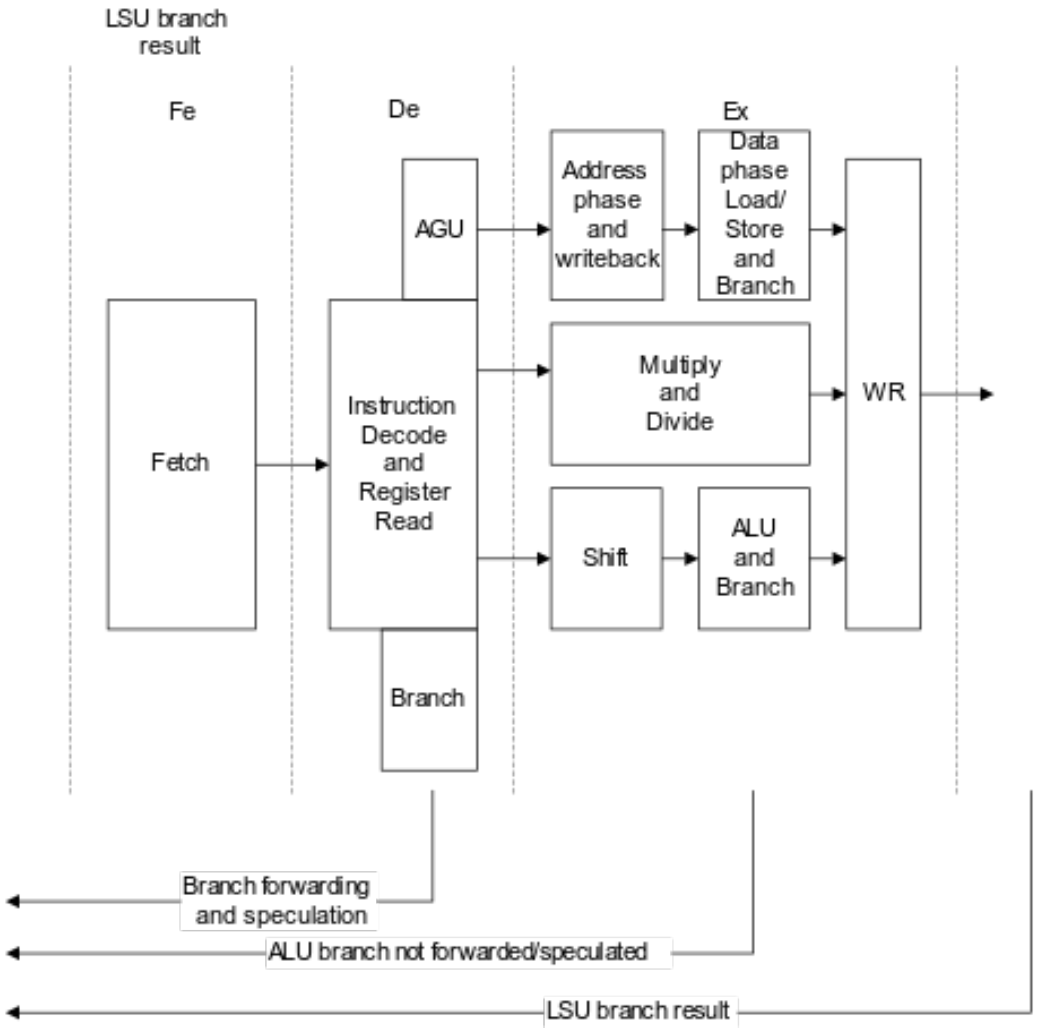


Figure 2.3: The 3-stage pipeline with Fetch, Decode & Execute
(Source : ARM® Infocenter)

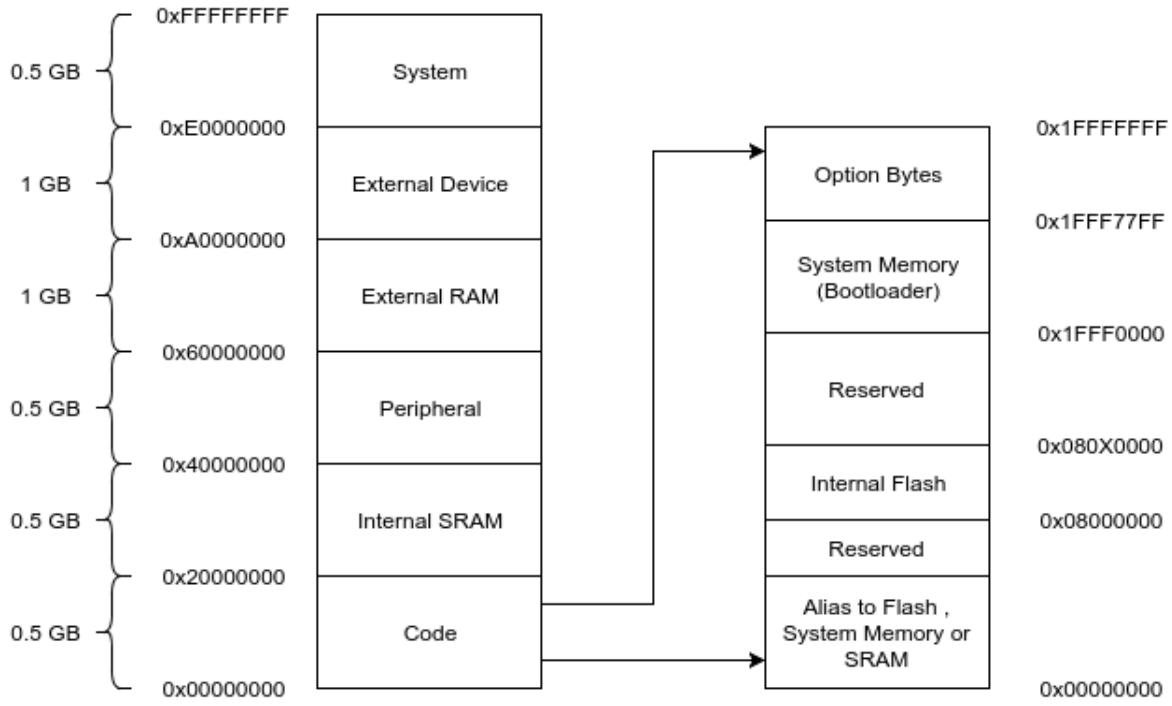


Figure 2.4: Peripheral & Memory organisation
(Source : ARM® Infocenter)

chosen as boot sector. Other options available are Internal SRAM and System Memory. The alias region maps the memory region for bootloading according to BOOT0 and BOOT1. The first word at 0x00000000 contains value of stack pointer which is loaded in SP and the second word at 0x00000004 contains address of *Reset_Handler()*. This address of *Reset_Handler()* is loaded to Program Counter. The *Reset_Handler()* function contains some initialisation functions along with *main()*. Subsequent addresses after 0x00000004 contains addresses of other routines which handle exceptions and other interrupts. This setting is done in the linker script.

The bootloader region of memory has the ability to write the internal flash memory so it can be used to upgrade the firmware.

2.2 Algorithm & Implementation

The algorithm implemented is shown in Figure 2.5. The optimised assembly subroutine is shown in Table 2.2. In Table 2.3, T_i represents the T-states of the processor core. The first instruction (*add r5,r0*) starts executing at T0, where at T0 it is fetched, in T1 it is decoded & at T2 it is executed. The second instruction (*lsr r6,r5,#20*) fetch occurs at T1 & while its decode & execute occurs at T2 & T3 respectively. As per the Technical Reference Manual of ARM Cortex M3, instructions *ldrh*, *str*, *ldr* take 2 machine cycles each. After T11, The pipeline is flushed & and the Program-Counter now points to instruction *add r5,r0*. It is fetched in next (T13). So effectively,

$$N = 12 \tag{2.4}$$

Sr. No	Function	Register
1.	Base address of short-int array	r4
2.	Frequency/Tuning register ($R_{frequency}$)	r0
3.	Phase Register (R_{phase})	r5
4.	Address of location for the content of $R_{frequency}$	r1
5.	Offset Register	r6
6.	Address of the GPIO Register	r2
7.	Temporary Register	r7

Table 2.1: Functions allocated to various registers

The *malloc()* function is used to allocate the array dynamically in SRAM during the first execution of the *main()* function. The base address of the array is retrieved from *malloc()* (present in *r0*) and moved to *r4* using (*mov r4,r1*) instruction.Whenever a new waveform is requested, it is either calculated using standard functions and stored to the array or transferred via USB using terminal in host PC. Some other functions allocated to other registers are mentioned in Table 2.1.

2.3 Schematic

The schematic featuring the ARM Micro-Controller-Unit (MCU) along with all necessary components connected is shown in Figure 2.6.

	.global sampler .equ GPIOA_ODR, 0x4001080C .extern freqRegisterContent

sampler :	mov r5,#0
	ldr r2, =GPIOA_ODR
	ldr r1, =freqRegisterContent

loop :	add r5,r0
	lsr r6,r5,#20
	lsl r6,r6,#1
	ldr r0,[r1]
	str r7,[r2]
	ldrh r7,[r4,r6]
	b loop
	nop

Table 2.2: Assembly subroutine in THUMB mode

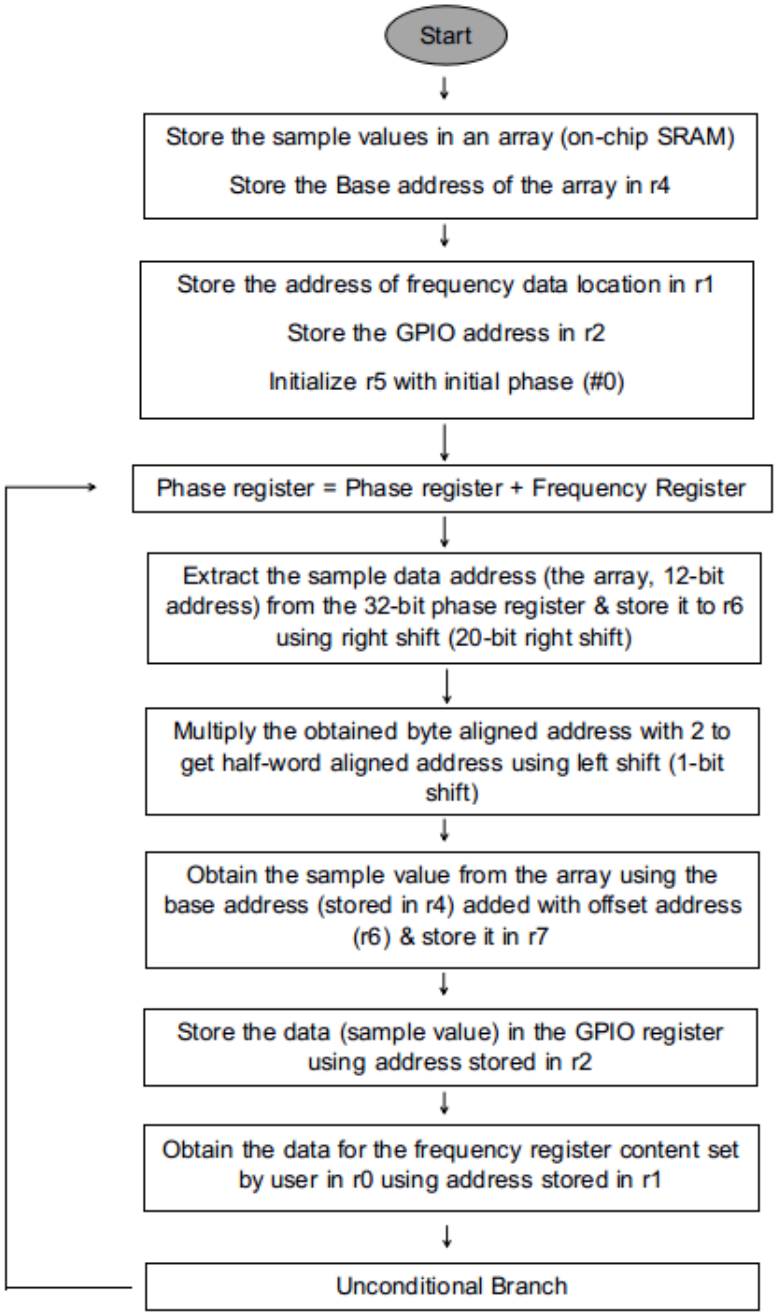


Figure 2.5: Algorithm Flow chart for the implementation of sampling subroutine

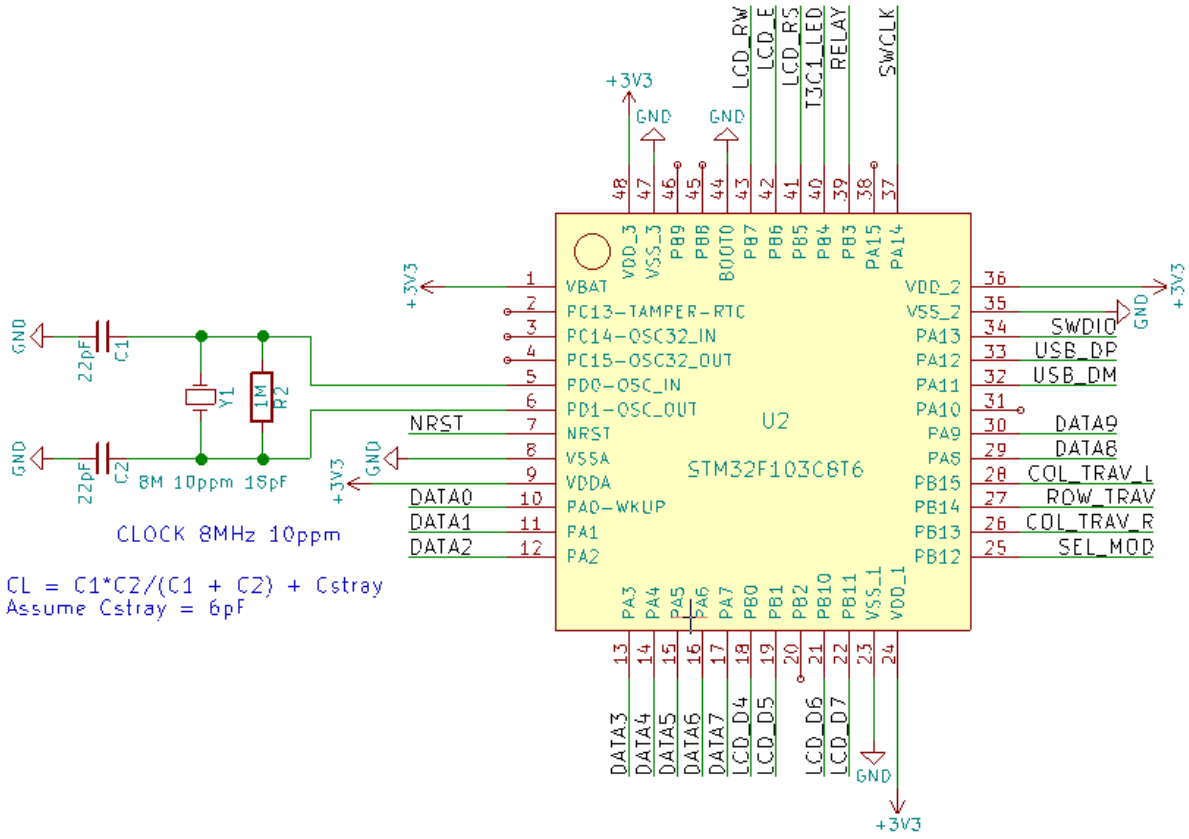


Figure 2.6: Circuit schematic of STM32F103C8T6 using KiCAD

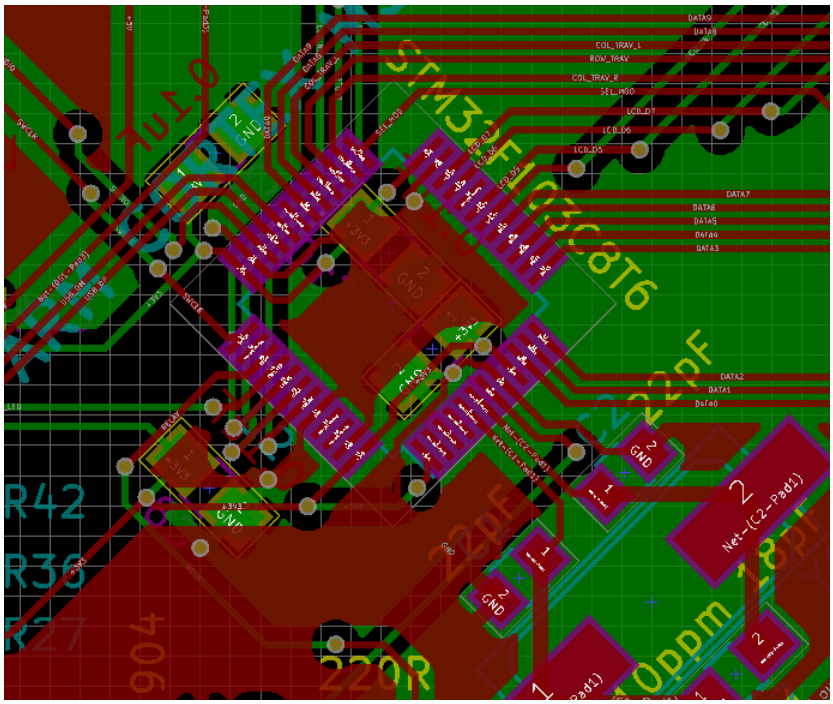


Figure 2.7: PCB layout of schematic shown in Figure 2.6

Instruction	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	T17
add r5,r0	F	D	E															
lsr r6,r5,#20		F	D	E														
lsl r6,r6,#1			F	D	E													
ldrh r7,[r4,r6]				F	D	E												
-					F	D	E											
str r7,[r2]						F	D	E										
-							F	D	E									
ldr r0,[r1]								F	D	E								
-									F	D	E							
b loop										F	D	E						
nop											F	D	-					
add r5,r0														F	D	E		
lsr r6,r5,#20															F	D	E	
lsl r6,r6,#1																F	D	E

Table 2.3: Anticipated Timing diagram of the assembly subroutine

Chapter 3

ANALOG SIGNAL PROCESSING

3.1 Basic concepts

The next step is conversion of digital signals from the GPIO pins to analog signals. This is achieved by a Digital to Analog Converters (DAC). A very simple architecture of DAC is R-2R ladder. It is a cost effective way to produce quality analog signals. The piecewise construction of the waveform contains harmonics due to phenomena $Zero^{th}$ Order Hold (Figure 3.2). This is a staircase response occurs due to convolution of sampling impulses (sequences of unit impulse function) with rectangle $(u(t) - u(t - T_{sampling}))$ in time domain. Actually $Zero^{th}$ order hold is a consequence not a cause. It occurs due to convolutional property in frequency domain [4]. According to Paley-Weiner criterion, these amplitudes of the harmonics in frequency spectrum cannot be eliminated completely , but can be attenuated considerably. Only non-causal signals can have brick wall response in frequency domain. The effects of unwanted frequency components can be minimised by following methods:

- Increasing the vertical resolution.
- Cascading a low pass filter.
- Both.

Filter is only required for sinosuidal waves, not for rectangular waves. This is because sine waves are bandlimited [4] (occurs at a point in frequency domain) while rectangular waves are not-bandlimited. This is achieved by bypassing the output of Digital to Analog converter using a DPDT signal relay. If filter is used for rectangular waves with frequency near to filter's cut-off frequency then due to non-linear phase response of the filter & attenuation of harmonics, the shape of rectangular wave deforms in time domain [7].

Now it is required to provide offset and gain as per the requirement of the user. This can be done using potentiometer and operational amplifiers. A high speed operational amplifier along with high current drive capability has been chosen for this purpose. Lastly a BNC is used which is preceded by a $\geq$ 500mW 50Ω resistance.

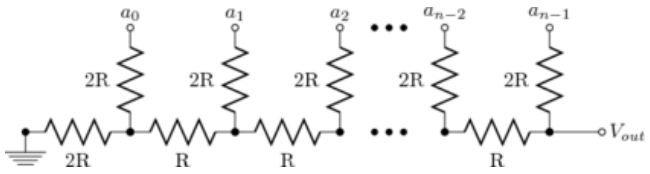


Figure 3.1: Digital to Analog converter : R-2R ladder

3.2 Direct Digital Synthesis

A DDS produces a sine wave at a given frequency [2]. The frequency depends on two variables, the reference-clock frequency ($F_{sampling}$) and the binary number programmed into the frequency register ($R_{frequency}$).

The binary number in the $R_{frequency}$ provides the main input to the phase accumulator R_{phase}. If a sine look-up table (implemented in SRAM) is used, the R_{phase} computes a phase (angle) address for the look-up table, which outputs the digital value of amplitude-corresponding to the sine of that phase angle to the DAC. The DAC, in turn, converts that number to a corresponding value of analog voltage or current. To generate a fixed-frequency sine wave, a constant value (the phase increment which is determined by the binary number) is added to the phase accumulator with each clock cycle. If the phase increment ($R_{frequency}$) is large, the phase accumulator will step quickly through the sine look-up table and thus generate a high frequency sine wave. If the phase increment is small, the phase accumulator will take many more steps, accordingly generating a slower waveform. This operation can be visualised using Figure 3.3.

3.2.1 Applications of DDS

Applications currently using DDS-based waveform generation fall into two principal categories: Designers of communications systems requiring agile (i.e., immediately responding) frequency sources with excellent phase noise and low spurious performance often choose DDS for its combination of spectral performance and frequency-tuning resolution. Such applications include using a DDS for modulation, as a reference for a PLL to enhance overall frequency tunability, as a local oscillator (LO), or even for direct RF transmission.

Alternatively, many industrial and biomedical applications use a DDS as a programmable waveform generator. Because a DDS is digitally programmable, the phase and frequency of a waveform can be easily adjusted without the need to change the external components that would normally need to be changed when using traditional analog-programmed waveform generators. DDS permits simple adjustments of frequency in real time to locate resonant frequencies or compensate for temperature drift. Such applications include using a DDS in adjustable frequency sources to measure impedance (for example in an impedance-based sensor), to generate pulse-wave modulated signals for micro-actuation, or to examine attenuation in LANs or telephone cables.

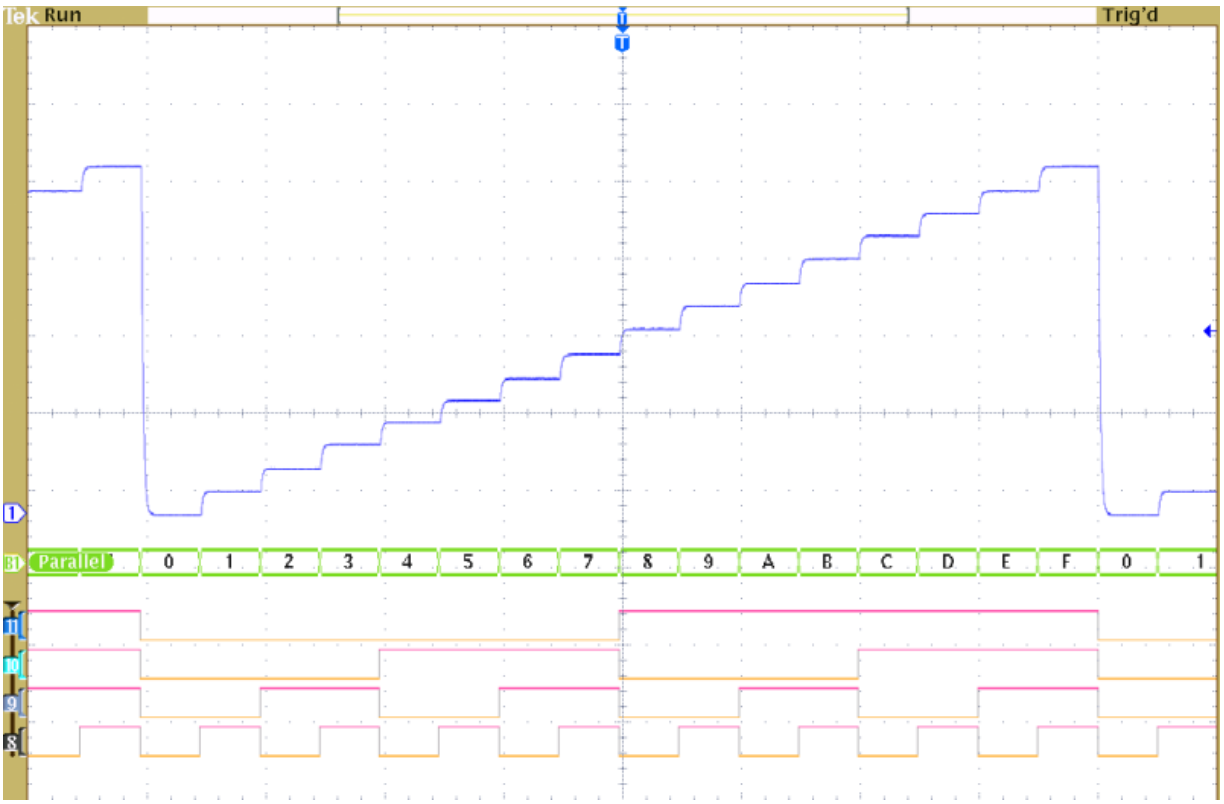
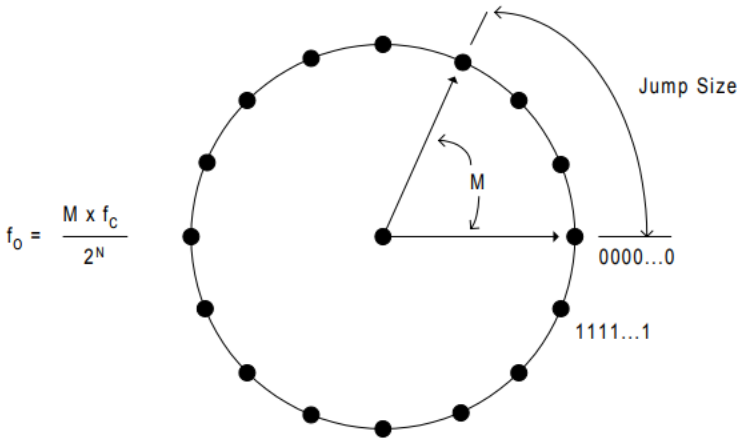


Figure 3.2: *Zero*th Order Hold
(Source : Tektronix Inc.)



n	NUMBER OF POINTS
8	256
12	4096
16	65535
20	1048576
24	16777216
28	268435456
32	4294967296

Figure 3.3: Visualisation of DDS operation using Diasy phase wheel
(Source : Analog Devices Inc.)

3.3 Digital to Analog Converter

There are several architecture of Digital to Analog Converters (DAC). Binary weighted DAC are common when it comes to its implementation on PCB. By methodical application of Thevenin Equivalent circuits and Superposition in Figure 3.1, it can be easily shown how the R-2R circuit works. The final expression for a 10-bit R-2R D/A converter,

$$V_{out} = \left(\frac{D_0}{2^{10}} + \frac{D_1}{2^9} + \frac{D_2}{2^8} + \frac{D_3}{2^7} + \frac{D_4}{2^6} + \frac{D_5}{2^5} + \frac{D_6}{2^4} + \frac{D_7}{2^3} + \frac{D_8}{2^2} + \frac{D_9}{2} \right) \tag{3.1}$$

The value of V_{ref} in the design is $3.3V$. We get the maximum output of the DAC $(V_{fullscale})$ when we have $D_n = V_{ref}$. It means that ,

$$V_{fullscale} = 3.3V \times \left(1 - \frac{1}{2^{10}}\right) \tag{3.2}$$

$$= 3.29677V \tag{3.3}$$

Major-Carry Transition - At the major-carry transition (around mid-scale), either the MSB changes from low to high and all other bits change from high to low, or the MSB changes from high to low and all other bits change from low to high. For example, 01111111 to 10000000 is a major-carry transition. Major-carry transitions often produce the worst switching noise.

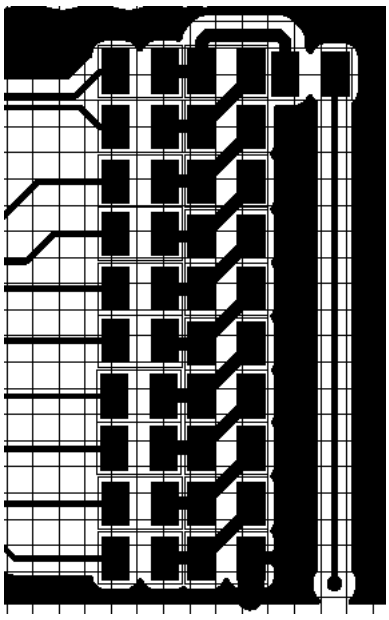


Figure 3.4: PCB layout of R-2R Digital to Analog Converter using 0805-SMD resistors

Offset Error - It is the analog output response to an input code of all zeros.

3.3.1 Disadvantages of R-2R ladder

R-2R DAC occupies large off-chip space in comparison to some other architectures available in integrated circuits. To achieve better time domain response (low settling time, rise time, fall time) low value resistors are recommended. This increases the power dissipation. If higher value resistors are used then it can suffer from thermal noise & poor transient response. It also suffers a lot from resistance mismatch. So it is recommended to use 1% tolerance resistance.

3.4 Gain & Offset : Operational-Amplifiers

The highest amplitude of the sine wave from the DAC is $3.3V$. The desired output amplitude has to be $5V$.

To achieve this task 2 stages of amplifiers have been used. It is shown in Figure 3.5. U1 and U4 are high-speed operational amplifiers with minimum specifications -

A	1 MEG
GBW	10 MEG
$SLEW$	100 V/μs
$Iout$	100 mA

Table 3.1: Minimum required specifications for High Speed Operational Amplifiers

To be cost effective, dual-operational amplifier LM7372/LM6172 from Texas Instruments® has been selected which provides more than sufficient features. These amplifiers have slew rate more than enough to support the rectangular waves. These provide gain & power to the output stage. Input to U1 which is applied at non-inverting pin using V4 is $(1.65+1.65\sin(\omega t))V$ & output from U1 is $3.3\sin(\omega t)V$. U4 is acting as power & gain amplifier, combining the offset from U2 & U3 (offset amplifiers) & user potentiometer (formed by R9 & R10) using superposition theorem. The linear function of offset potentiometer varies from $(0V, 3.3V)$, is mapped to $(-5.0V, +5.0V)$ using U2 & U3. It is being implemented using LM358 from Texas Instruments®.

A	1 MEG
GBW	1 MEG
SLEW	0.6 V/μs
Iout	20 mA

Table 3.2: Specifications for General Purpose Operational Amplifiers (LM358)

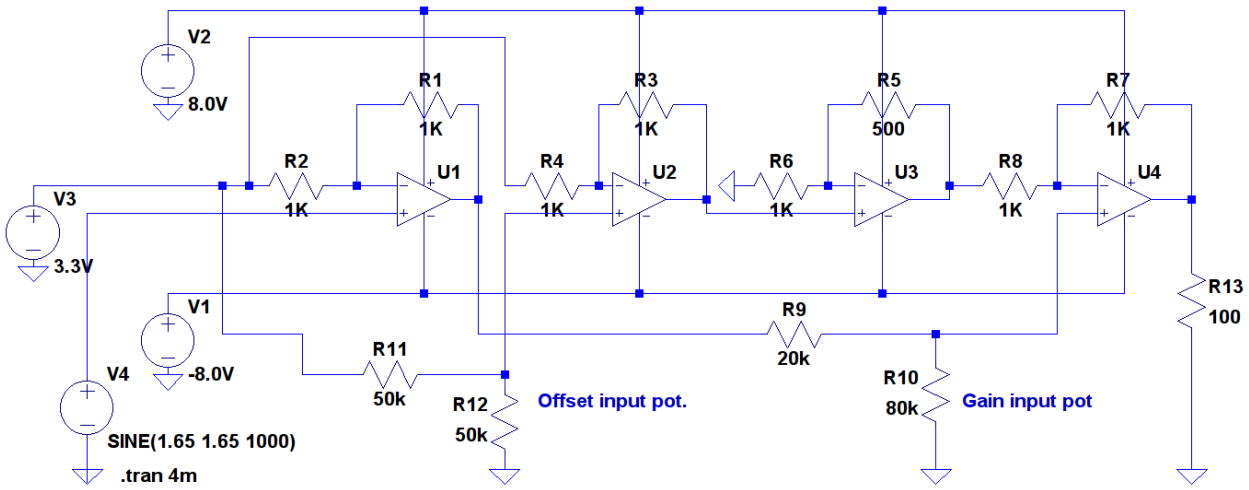


Figure 3.5: Gain and Offset circuit

3.5 Filter

The problem due to $Zero^{th}$ Order Hold (Figure 3.2) can be minimised using a RLC low pass filter [7] , [5]. A low pass filter with 3-dB cut-off frequency at 1 MHz has been designed using RLC filter. It is utilized to attenuate the image responses in the output spectrum due to sampling. In order to keep the cutoff requirements on the lowpass filter reasonable, it is an accepted rule to limit the F_{out} bandwidth to approximately 40% of the $F_{sampling}$.

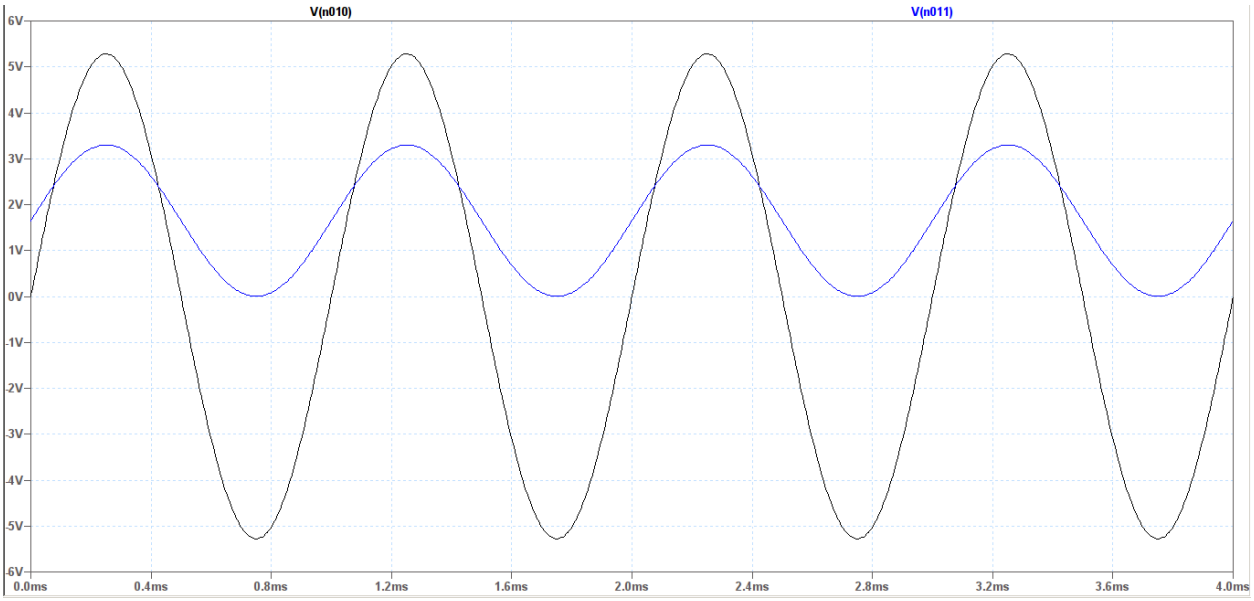


Figure 3.6: Simulation Result for Figure 3.5

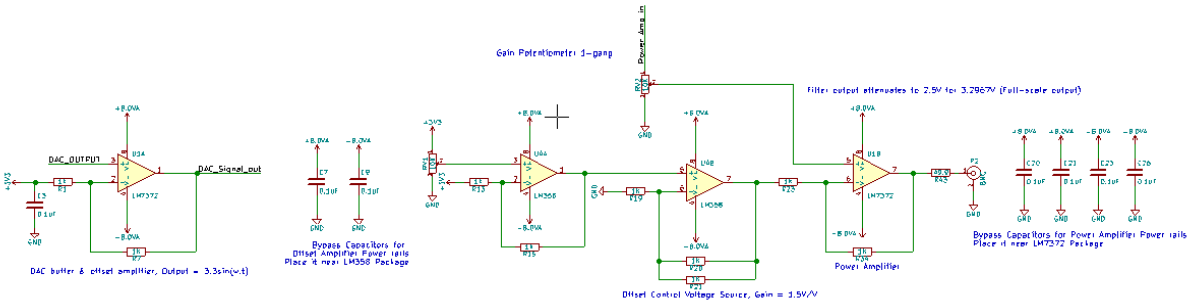


Figure 3.7: Actual schematic design in KiCAD

Using Equation (1.5), Substituting $F_{pll} = 72MHz$ & $N = 12$,

$$F_{sampling} = \frac{72MHz}{12} \tag{3.4}$$

$$F_{sampling} = 6.000MHz \tag{3.5}$$

The design goal frequency = 1 MHz (Table 1.1) which is $\approx 20\%$ of the $F_{sampling}$ well below the Nyquist frequency $\left(\frac{F_{sampling}}{2}\right)$.

A single RLC filter was designed for the first time. To achieve faster roll-off in frequency domain, 2 more stages were cascaded. It is now clear that the resulting filter will suffer from loading effect & will start rolling off before the desired cutoff frequency in frequency domain. To mitigate this error a reliable simulation tool (LTspice) has been used to verify & tune the parameters. It was also required to have uniform component values. R = 50Ω has been chosen to limit the current in

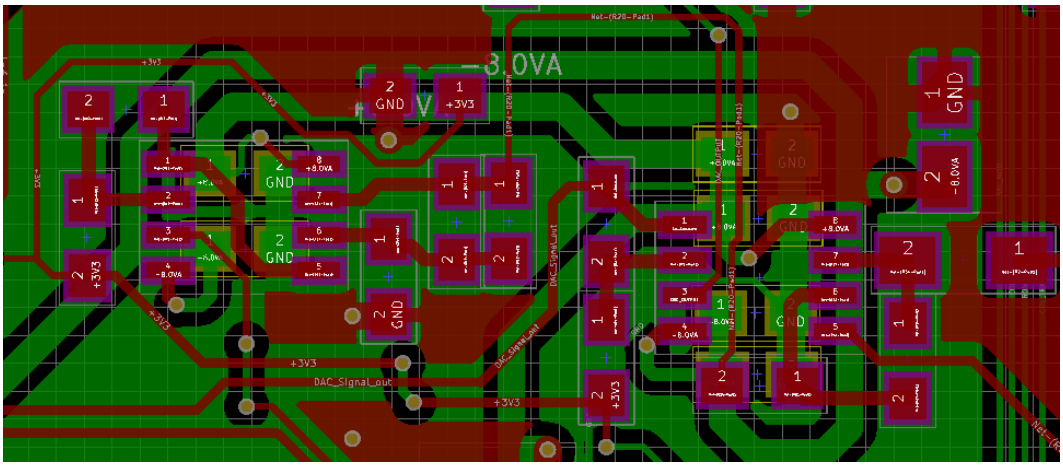


Figure 3.8: PCB layout of the designed circuit in Figure 3.7

time domain & peaking in frequency domain (to achieve near over-damped response). It is important to limit the current so that it comes under tolerable range of the inductor current specifications, should be $\leq I_{saturation}$.

Cutoff frequency of a single stage RLC circuit is :

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{3.6}$$

$$C = \left(\frac{1}{2\pi \times f_c}\right)^2 \times \frac{1}{L} \tag{3.7}$$

$$C = \left(\frac{1}{2\pi \times 1000000}\right)^2 \times \frac{1}{10\mu H} \tag{3.8}$$

$$C = 2533pF \tag{3.9}$$

From (3.9) , the value of C is found to be 2533 pF.

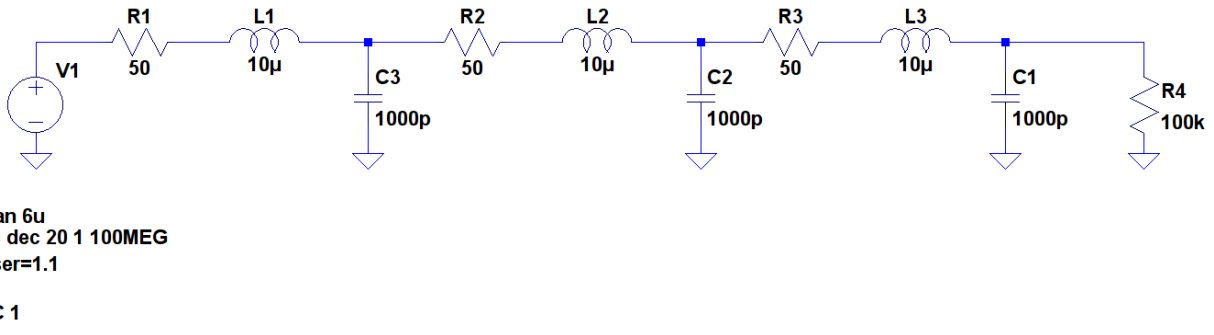


Figure 3.9: RLC Low pass filter

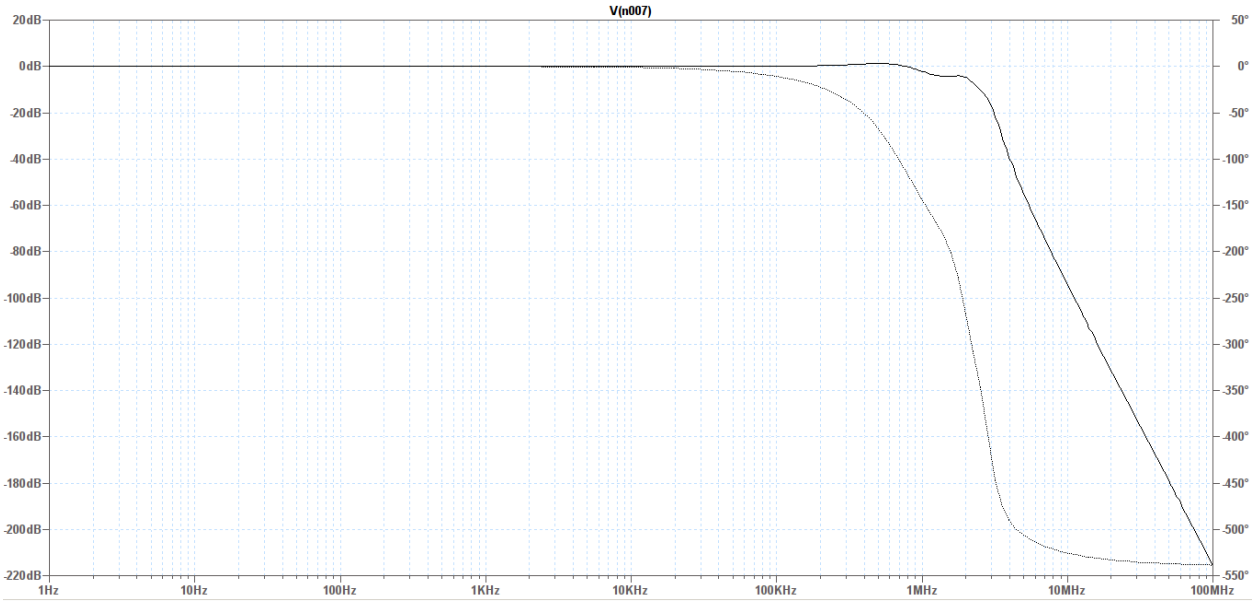


Figure 3.10: Frequency Response of the filter mentioned in Figure 3.9

The frequency response is shown in Figure 3.10. The solid line represents amplitude response & and dashed line represents phase response. Since we are designing a single channel waveform generator we can ignore the phase response. The approximate rolloff rate is -200 dB/decade. It is justified by the transient responses in Figure 3.11 & Figure 3.12, where output almost vanishes for 5 MHz input.

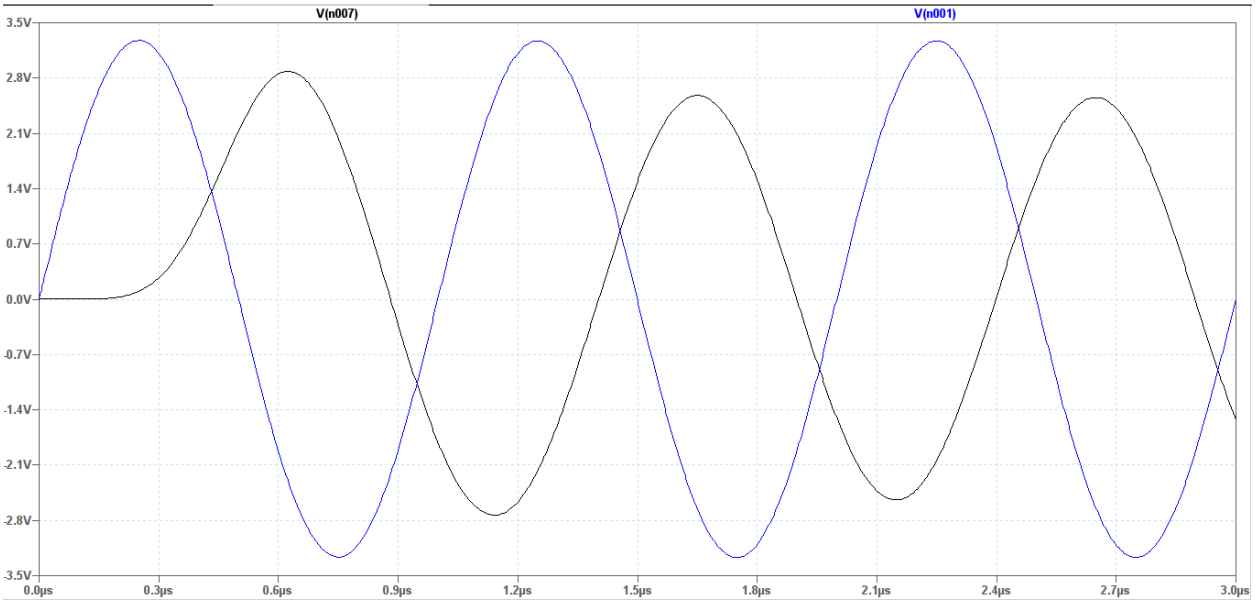


Figure 3.11: Transient analysis of the filter at input frequency 1 MHz & Amplitude 3.3 V

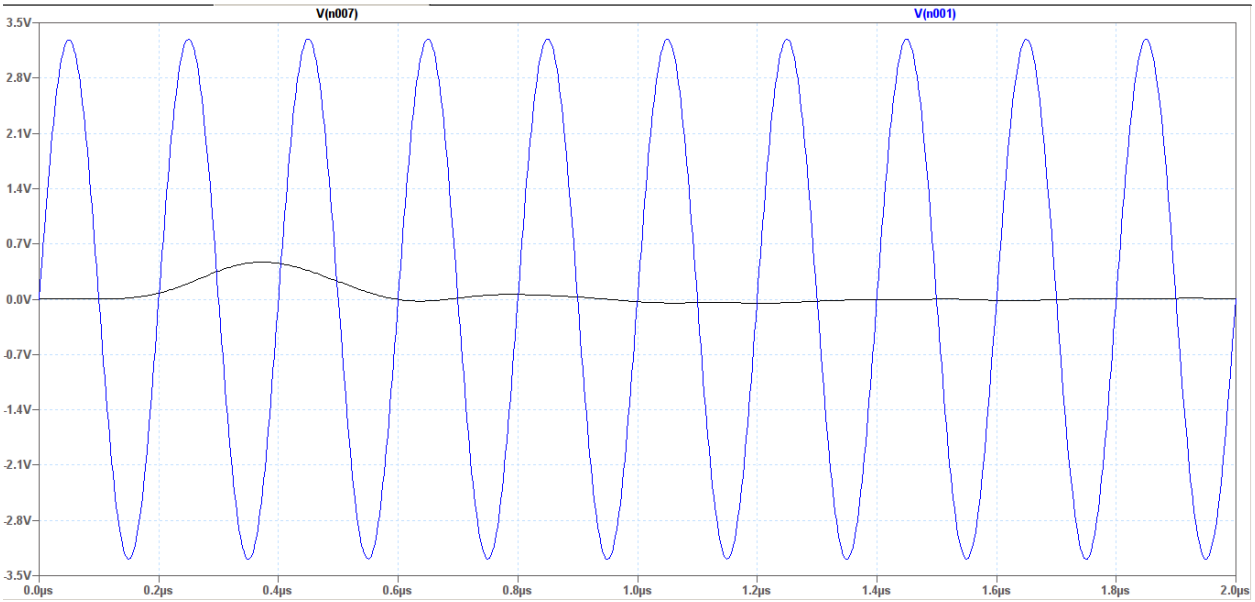


Figure 3.12: Transient analysis of the filter at input frequency 5 MHz & Amplitude 3.3 V

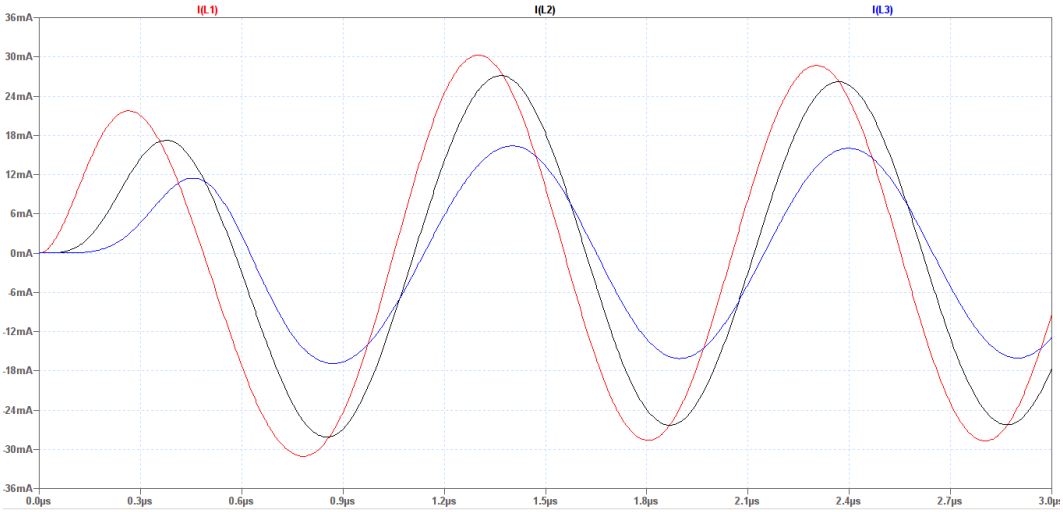


Figure 3.13: Current inside the Inductors

It is clear from Figure 3.13 that the maximum current does not exceed 30 mA, so we can choose inductors with sufficient $I_{saturation}$. Wire-wound chip inductors from Taiyo-Yuden (LB2016T100M) having rated current at 155 mA has been chosen for this application.

Chapter 4

POWER SUPPLY UNIT

4.1 Basic Requirements

The output of the operational-amplifiers can go from $-5V to +5V$. The power is derived from the USB which provides $V_{bus} = +5V$. Operational-Amplifiers LM7372/LM6172 have headroom & legroom of approximately 2V. So it is required to have power rails of $\pm 7V$. Further 1V is added as safe margin. Therefore the final requirement is $\pm 8V$. Both the voltage (input & output) are DC so it require DC to DC converter. To get a output of $+8V$ from $+5V$, a boost converter is required. A inverter is required for $-8V$ conversion from $+5V$.

4.2 Switching Regulators

There are basically 2 types of voltage regulators namely linear voltage regulators & switching voltage regulators. Linear voltage regulators are connected in parallel or series which can vary the resistance across it to regulate the voltage. Switching regulators use semiconductor switching techniques, rather than standard linear methods to provide the required output voltage. Switching regulators are more power efficient & dissipate very less heat. Linear regulators cannot step-up voltage so it cannot be used in boost applications.

The most basic switching topology only require a transistor which is essentially used as a switch, one diode, one inductor, a capacitor across the output, and for practical but not fundamental reasons, another one across the input. A practical converter, however, requires a control section comprised of several additional elements, such as a voltage reference, error amplifier, comparator, oscillator, and switch driver, and may also include optional features like current limiting and shutdown capability.

Any DC to DC converter having feedback do have the capability to regulate the output voltage. So it is now called regulator. From now term **regulators** would be used in place of **converters** because the IC used in design has feedback to regulate the output.

There are basically 3 types of switching regulator namely Buck, Boost & Invert. If the output

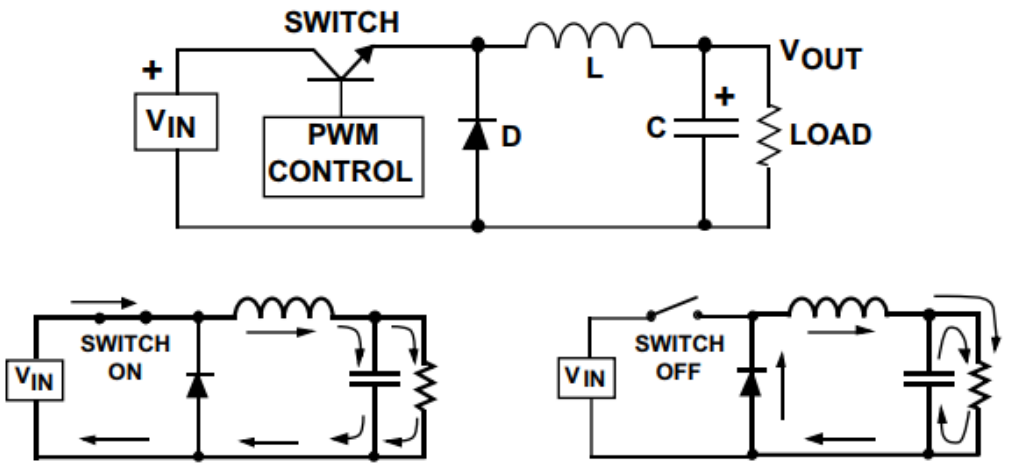


Figure 4.1: Buck switching regulator
(Source : Texas Instruments Inc.)

voltage is less than input voltage in magnitude then it is buck regulator (Figure 4.1). If the output voltage is greater than input voltage in magnitude then it is boost regulator (Figure 4.2). If the input voltage is positive & output voltage is negative then it is inverting switching regulator (Figure 4.3).

For this design, only inverting & boost topology is required. MC34063 [6],[1] from Texas Instruments is used to implement these topologies.

4.3 Calculations

Calculations required to determine the off-chip component values of MC34063 [1] are mentioned in Table 4.1. Fundamental concepts of inductors, capacitors, diode, BJT/MOS Switches & the waveforms shown in Figure 4.4 & Figure 4.5 are key to develop the relations required for the component value calculation [6].

When Switch is ON (Boost topology),

$$I_{inductor} = \frac{V_{in} - V_{sat}}{L} \times t \tag{4.1}$$

When Switch is OFF (Boost topology),

$$I_{inductor} = I_{inductor(peak)} - \frac{V_{out} - V_F - V_{in}}{L} \times t \tag{4.2}$$

In discontinous mode, the $I_{inductor(peak)}$ which flows from switch during t_{on} should decay to 0 through the schottky diode during t_{off}.

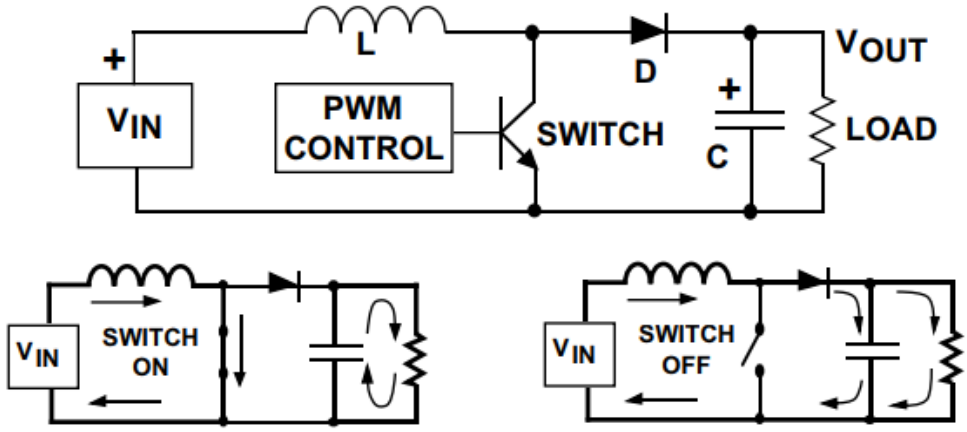


Figure 4.2: Boost switching regulator
(Source : Texas Instruments Inc.)

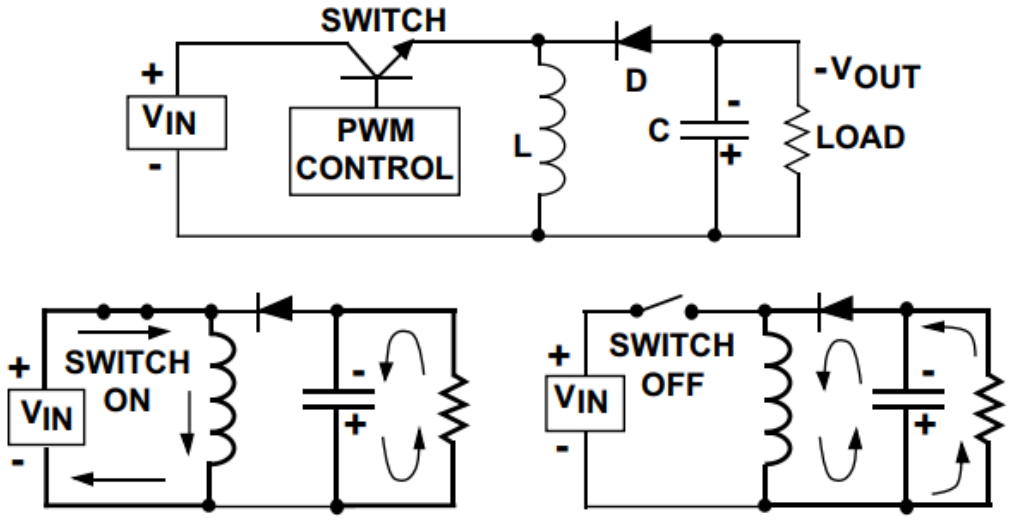


Figure 4.3: Inverting switching regulator
(Source : Texas Instruments Inc.)

Time ON & OFF calculation (Boost topology),

$$\frac{t_{on}}{t_{off}} = \frac{V_{out} + V_F - V_{in}}{V_{in} - V_{sat}} \tag{4.3}$$

Time ON & OFF calculation (Inverter topology),

$$\frac{t_{on}}{t_{off}} = \frac{|V_{out}| + V_F}{V_{in} - V_{sat}} \tag{4.4}$$

Peak current calculation,

$$I_{inductor(peak)} = 2I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right) \tag{4.5}$$

Inductance calculation,

$$L_{min} = \left(\frac{V_{in} - V_{sat}}{I_{peak(switch)}}\right) \times t_{on(max)} \tag{4.6}$$

Timing capacitor calculation,

$$C_{timing} = 4 \times 10^{-5} \times t_{on} \tag{4.7}$$

Output Capacitor calculation,

$$C_{out} = \frac{9I_{out}t_{on}}{V_{ripple(pp)}} \tag{4.8}$$

Property	Boost	Inverter
Requirements & Given data	$V_f(B340A) = 0.5V$, $I_f = 3A$, $T_j = 25\deg C$	$V_f(B340A) = 0.5V$, $I_f = 3A$, $T_j = 25\deg C$
	$I_{out} = 150mA$, $V_{out} = +8.0V$	$\|I_{out}\| = 150mA$, $V_{out} = -8.0V$
	$V_{in} = +5V \pm 10\%$	$V_{in} = +5V \pm 10\%$
	$V_{ripple(pp)} = 25mV_{pp}$	$V_{ripple(pp)} = 25mV_{pp}$
	$V_{sat} = 0.45V$, Non-darlington	$V_{sat} = 1.0V$, Darlington
Calculations & Result	$t_{on} = 4.3052\mu s$, $t_{off} = 5.6947\mu s$	$t_{on} = 6.7742\mu s$, $t_{off} = 3.2261\mu s$
	$C_{timing} = 172.0pF$	$C_{timing} = 270.9pF$
	$I_{inductor(peak)} = 0.5628A$	$I_{inductor(peak)} = 0.93A$
	$L_{min} = 37.18\mu H$	$L_{min} = 33.14\mu H$
	$C_{out} = 232\mu F$	$C_{out} = 365\mu F$
	$R_{sc} = 0.626\Omega$	$R_{sc} = 0.354\Omega$

Table 4.1: Calculations required for switching regulator MC34063

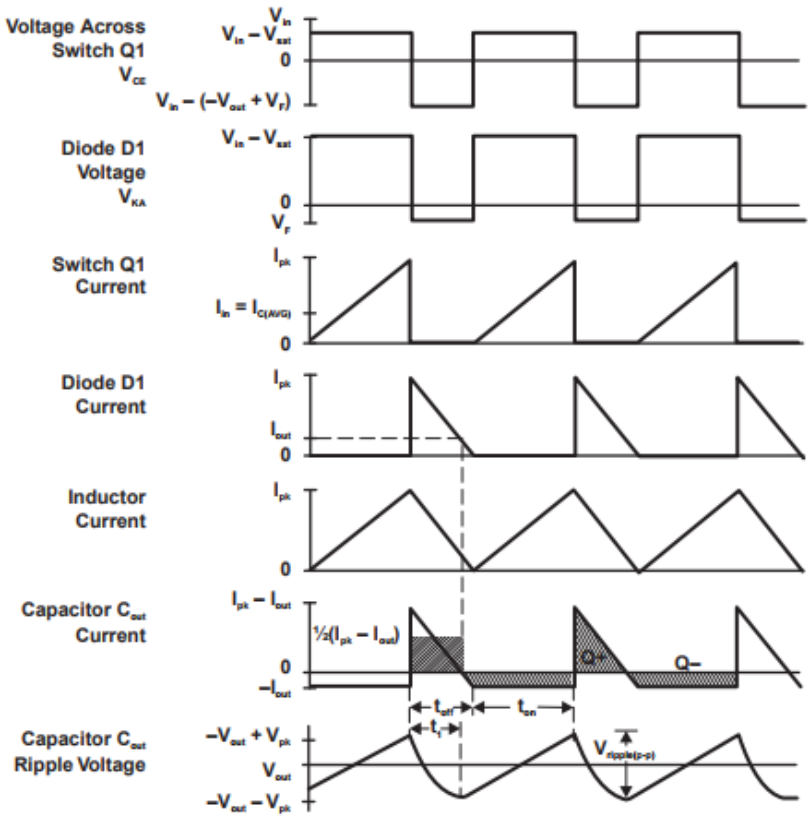


Figure 4.4: Inverting switching regulator waveform
(Source : Texas Instruments Inc.)

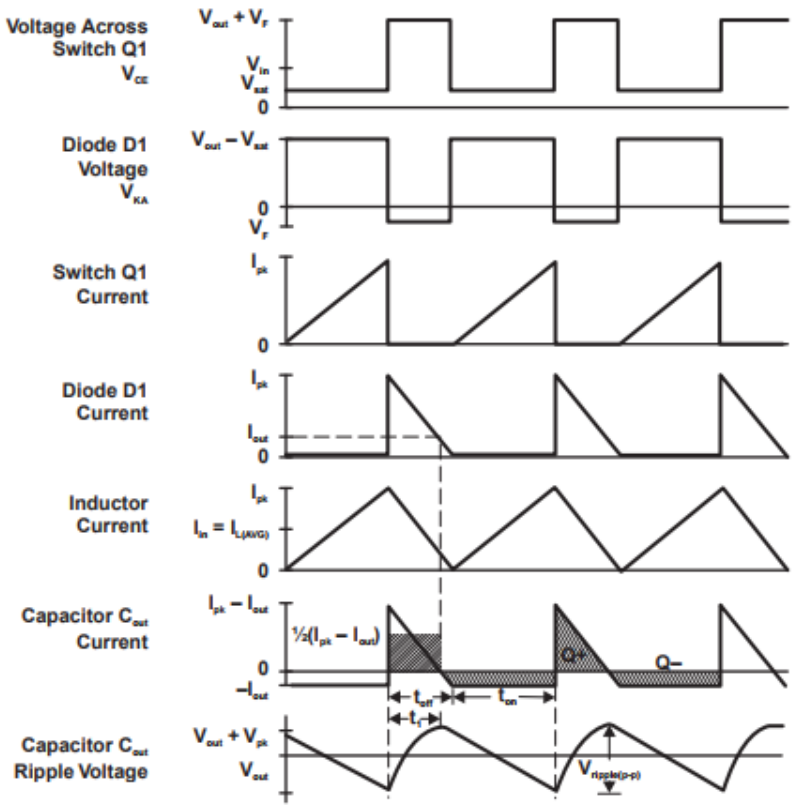


Figure 4.5: Boost switching regulator waveform
(Source : Texas Instruments Inc.)

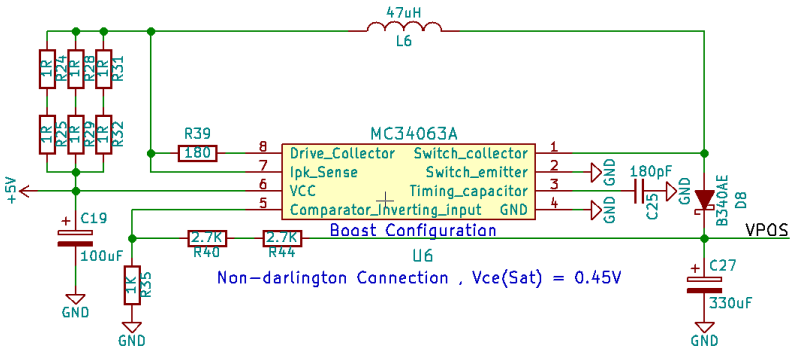


Figure 4.6: Circuit implemented using MC34063 in KiCAD : Boost topology

4.4 Circuit Design

The circuit schematic is shown in Figure 4.6 & Figure 4.8. The traces have been kept short to minimise ESR and parasitic effects while keeping the traces wide enough to handle peak currents. Semi-shielded power inductors from BOURNS® have been used as these are medium priced components with better EMI performance than non-shielded counter-parts. Ground traces are kept short to minimise current loop. Ground has been provided through vias to the ground plane (Back layer).

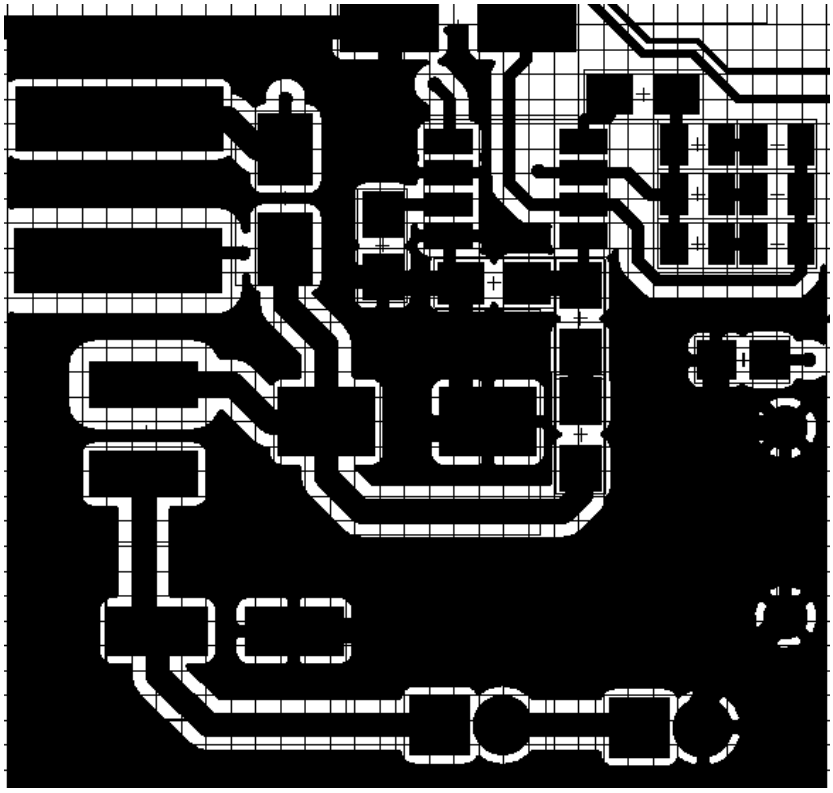


Figure 4.7: PCB layout of the schematic in Figure 4.6, (Not to scale)

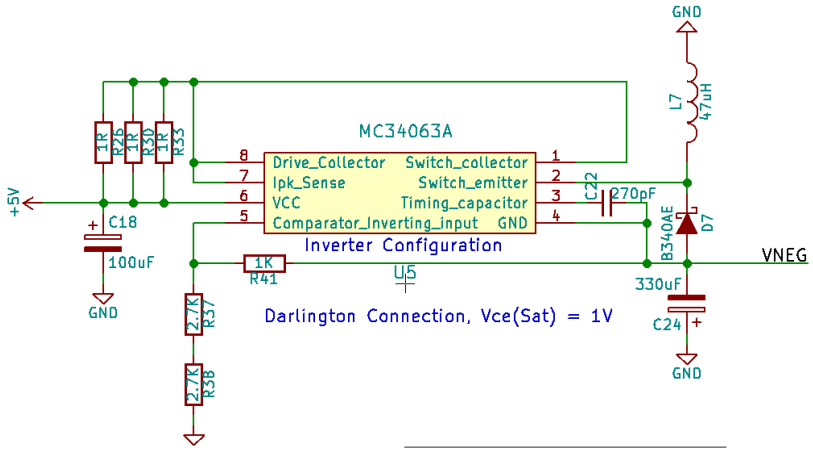


Figure 4.8: Circuit implemented using MC34063 in KiCAD : Inverter topology

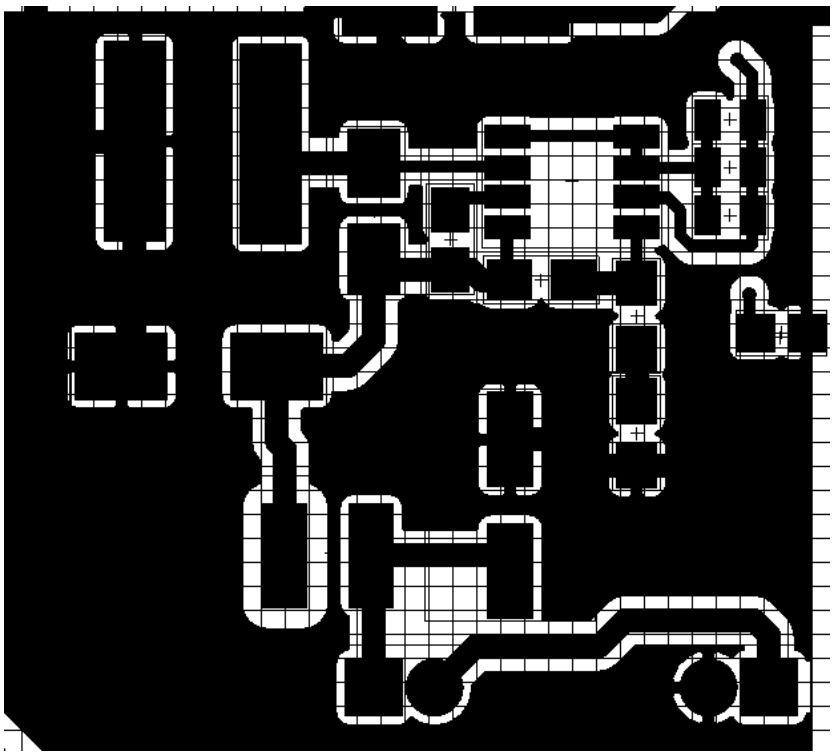


Figure 4.9: PCB layout of the schematic in Figure 4.8, (Not to scale)

Chapter 5

DESIGN & DEVELOPMENT TOOLS

5.1 Embedded Development

Embedded Software design require a lot of tools at once for writing code, code-correction, De-referencing declarations, tool-chain configuration, downloading code to MCU, debugging and many more. It is required that every non-essential detail is abstracted from developer & he/she mainly focuses on developing the software. So an Integrated Development Environment (IDE) is required.

Atollic TrueSTUDIO 8.0.0 is used here for developing embedded software for STM32F103. The free version is having advanced debugging features like registers & SFRs view, step-mode diassembly, memory browser etc. A glimpse of the environment is shown in Figure 5.2.

For debuging ST-LINK V2 is used which supports Serial Wire Debug (SWD) interface. This type of debugger is very useful while developing such a advanced core like ARM Cortex M3. It allows to stop the core & extract a snapshot of the entire processor whenever required using either breakpoints or using the pause function of IDE.

5.2 PCB Design

KiCAD is used here for the Printed Circuit Board (PCB) designing. It is open-source tool for schematic capture, component selection, PCB layout & design. It has integrated gerber viewer for viewing the files sent to manufacturer.

1. KiCad - the project manager.
2. Eeschema - the schematic capture editor.
3. Pcbnew - the PCB layout program. It also has a 3D view.
4. GerbView - the Gerber viewer.
5. Bitmap2Component - tool to convert images to footprints for PCB artwork

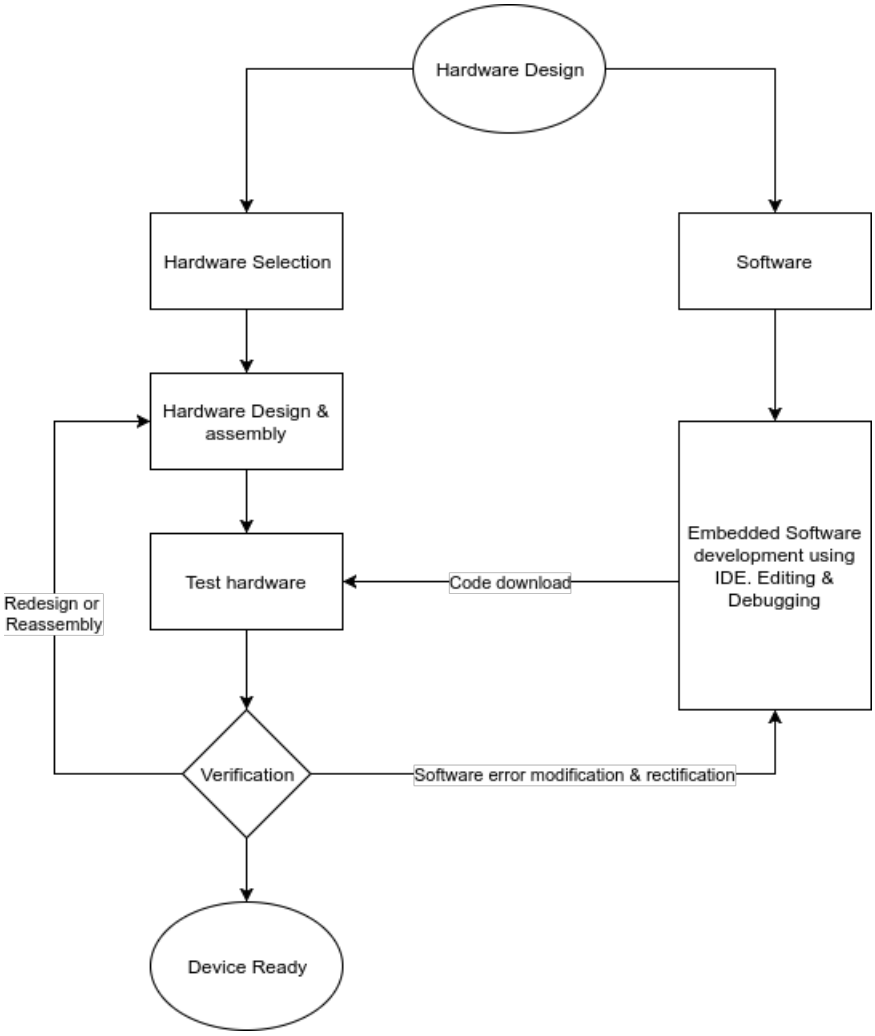


Figure 5.1: Hardware Development Cycle flow chart

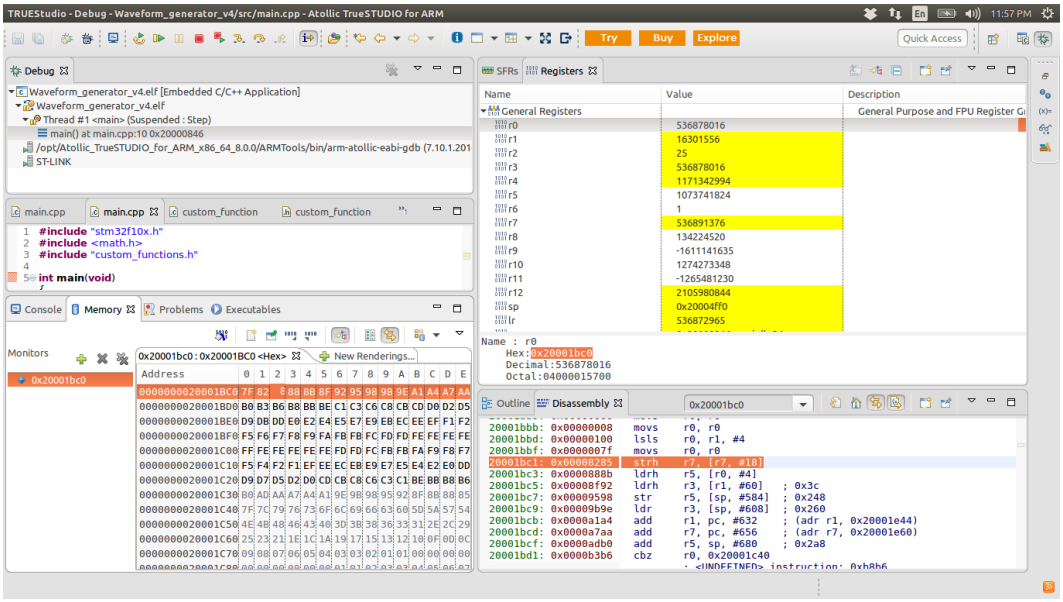


Figure 5.2: Debugging in Atollic TrueSTUDIO IDE

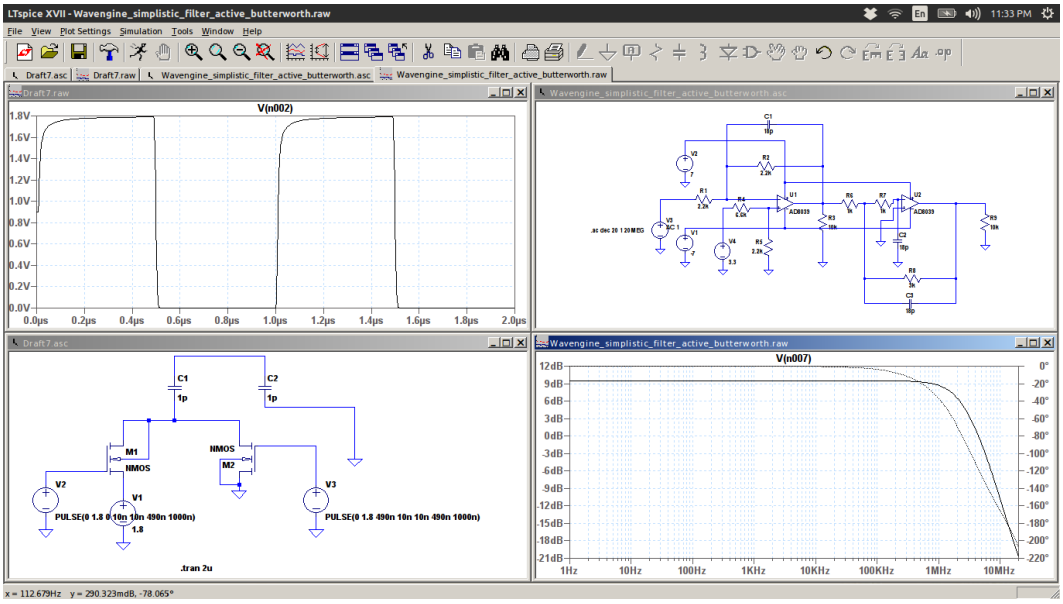


Figure 5.3: Simulation using LTSpice

5.3 SPICE - Non-Linear Simulator

Simulation Program with Integrated Circuit Emphasis (SPICE) is a general-purpose board level circuit simulation program for nonlinear dc, nonlinear transient, & linear ac analyses. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, lossless and lossy transmission lines (two separate implementations), switches, uniform distributed RC lines, and the five most common semiconductor devices: diodes, BJTs, JFETs, & MOSFETs. SPICE originates from the EECS Department of the University of California at Berkeley.

LTspice from Linear Technology (Now a part of Analog Devices Inc.) is used here for board level simulation. It is a freeware program having all the necessary tools required for circuit simulation. The results are consistent with practical circuits if all the parameters including parasitics are considered. The tool proves to be very useful when calculating responses of a mathematically complicated filter circuit shown in Figure 3.9. A workspace screen shot has been shown in Figure 5.3.

5.4 Mathematical computation

MATLAB is occassionaly used to match practical output with principles in theory.

5.5 Bill of Materials

The Bill of materials is shown in Table 5.1.

Sr. No	Manufacturer	Manufacturer Part Number
1.	TEXAS INSTRUMENTS	LM6172IM/NOPB
2.	ON SEMICONDUCTOR	MMBT3904
3.	STMICROELECTRONICS	LM358DT
4.	TEXAS INSTRUMENTS	MC34063ADE4
5.	MOLEX	105017-0001
6.	YAGEO (PHYCOMP)	RC0805FR-07220RL
7.	MULTICOMP	MC0805N271J500CT
8.	KEMET	C0805C220J5GACTU
9.	KEMET	C0805C104K5RACTU
10.	MULTICOMP	MC0805N181J500CT
11.	BOURNS	SRN5040-100M
12.	BOURNS	PTV09A-4020U-B104.
13.	MULTICOMP	MCWR08X1001FTL

Table 5.1 continued from previous page

Sr. No	Manufacturer	Manufacturer Part Number
14.	MULTICOMP	MCWR08X2001FTL
15.	MULTICOMP	MCWR08X2701FTL
16.	MULTICOMP	MCWR08X1501FTL
17.	MULTICOMP	MCWR08X1200FTL
18.	PANASONIC ELECTRONIC COMPONENTS	ERJ-6ENF6040V
19.	NICHICON	UWX1C101MCL1GB
20.	NICHICON	UWX1C100MCL2GB
21.	NICHICON	UWT1C331MNL1GS
22.	TAIYO YUDEN	LB2016T100M
23.	YAGEO (PHYCOMP)	CC0805ZRY5V9BB104
24.	YAGEO (PHYCOMP)	CC0805KRX7R9BB102
25.	BOURNS	SRN8040-470M
26.	DIODES INC.	B340A-13-F
27.	KEMET	T491A106M016AT
28.	KEMET	T491A475K025AT
29.	TE CONNECTIVITY / AXICOM	V23105A5001A201
30.	PANASONIC ELECTRONIC COMPONENTS	ERJP08F49R9V
31.	MULTICOMP	MC0805S8F1800T5E
32.	MULTICOMP	MCWR08W1R00FTL
33.	MULTICOMP	MCWR08X4701FTL
34.	TXC	9C-8.000MEEJ-T
35.	MULTICOMP	MCWR08X1202FTL
36.	TAIWAN SEMICONDUCTOR	TS1117BCW-3.3
37.	STMICROELECTRONICS	STM32F103C8T6
38.	CRYSTALFONTZ	CFAH1602A-YYH-JT
39.	MULTICOMP	13-22-1

Table 5.1: Bill of Materials

Chapter 6

RESULTS & EVALUATION

6.1 PCB layout

The schematic has been designed in KiCAD and shown in Figure 6.1. The final PCB layout corresponding to schematic in Figure 6.1 is shown in Figure 6.2 & 6.3.

6.2 Prototype

The breadboard prototype of the design is shown in Figure **??**. Final PCB assembled prototype is also shown in Fig 6.6. Keysight DSO1052B is used to observe the waveforms. ADATA PT100 Power Bank is used to provide +5V power supply.

6.3 3D rendered view

The 3D view of the design is shown in Figure 6.5.

6.4 Waveforms

Waveforms produced from the prototype are mentioned in Figure 6.7 to Figure 6.12.

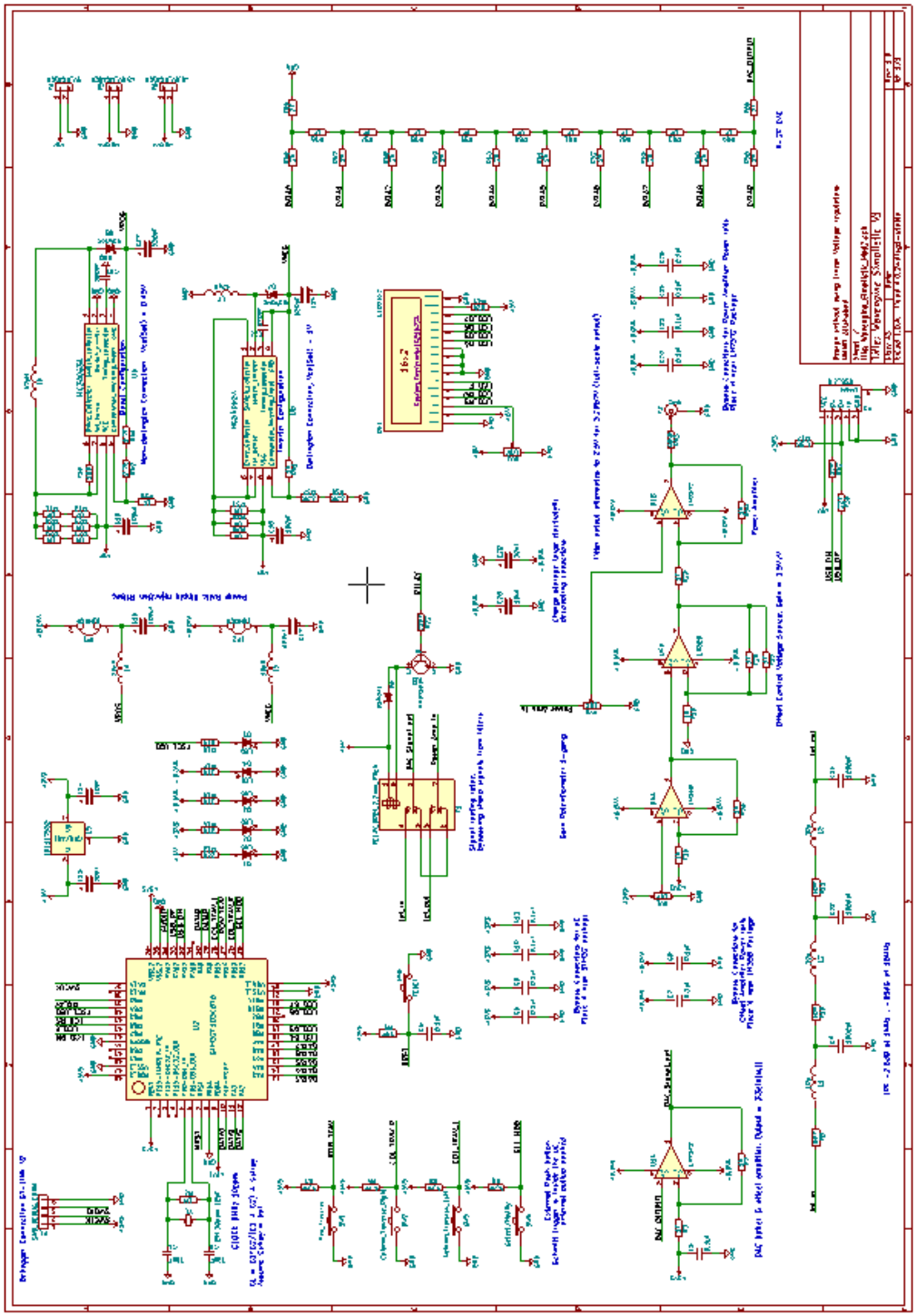


Figure 6.1: Schematic of the entire design in KiCAD

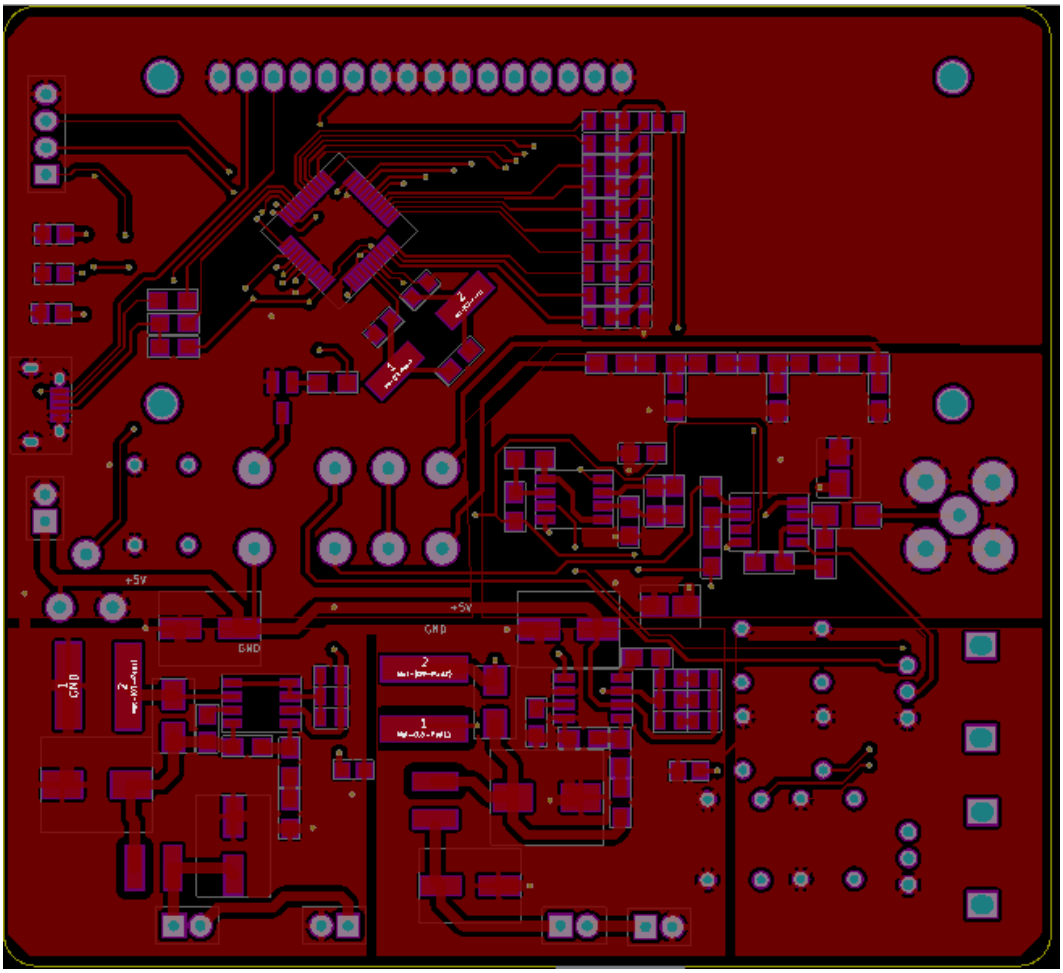


Figure 6.2: PCB layout - Front layer

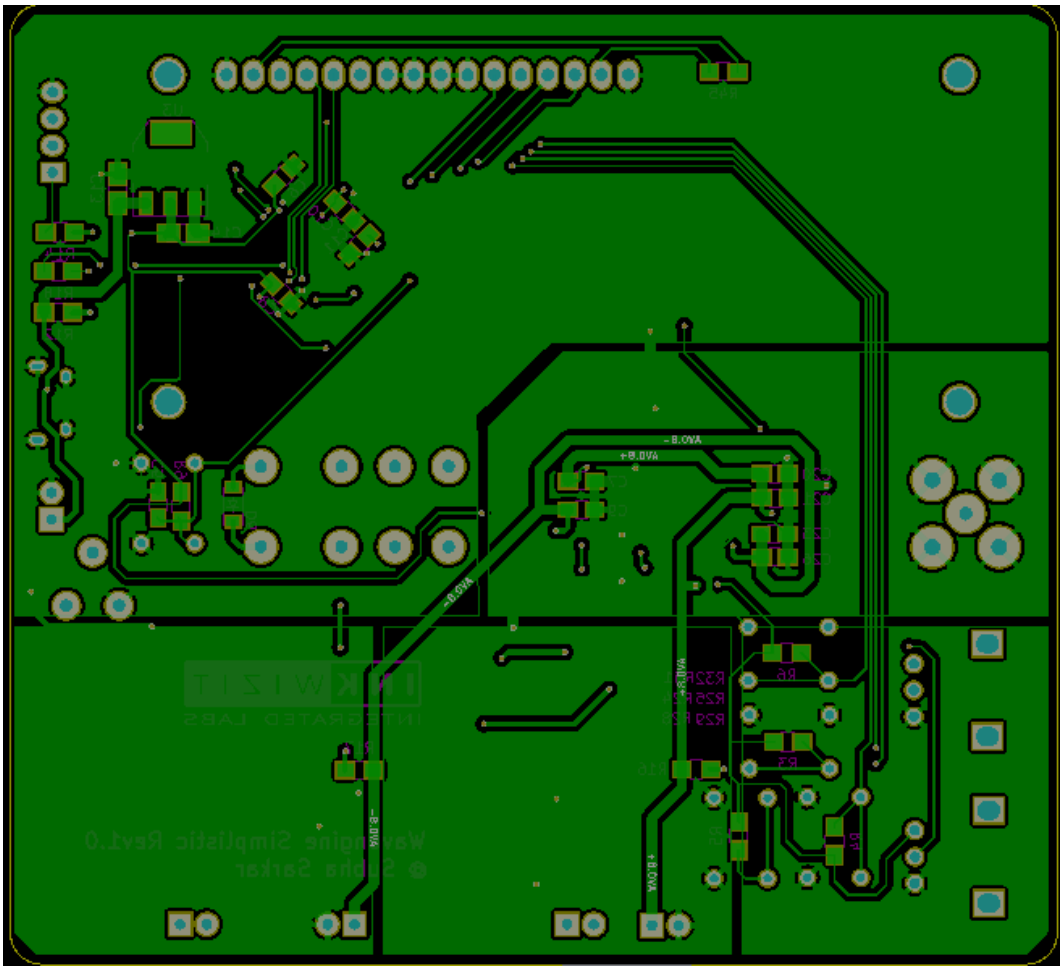


Figure 6.3: PCB layout - Back layer

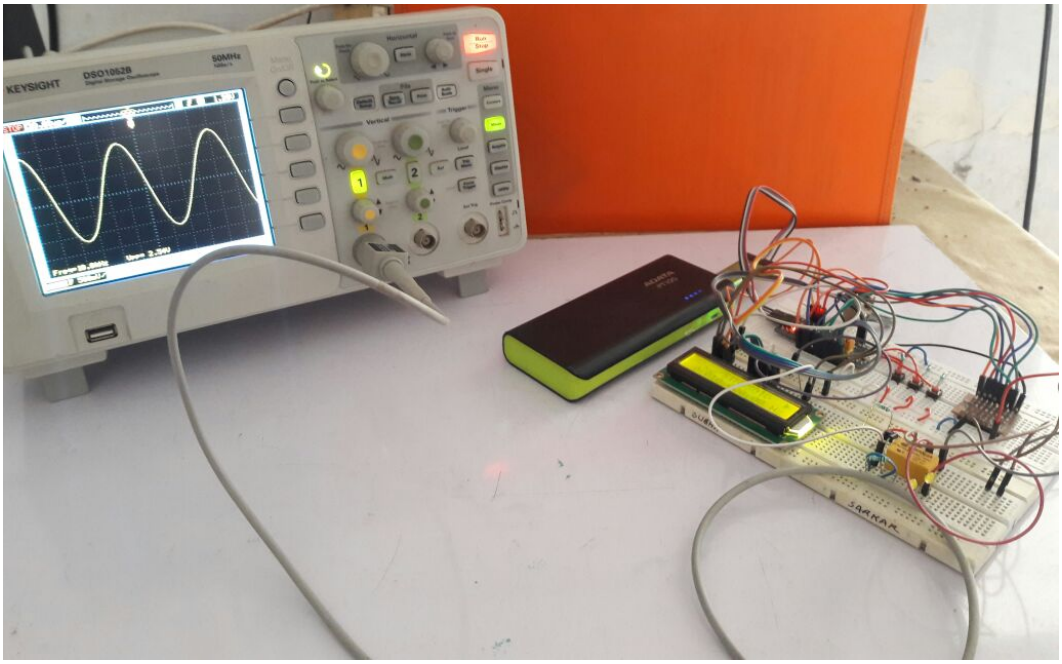


Figure 6.4: Version 2 prototype working

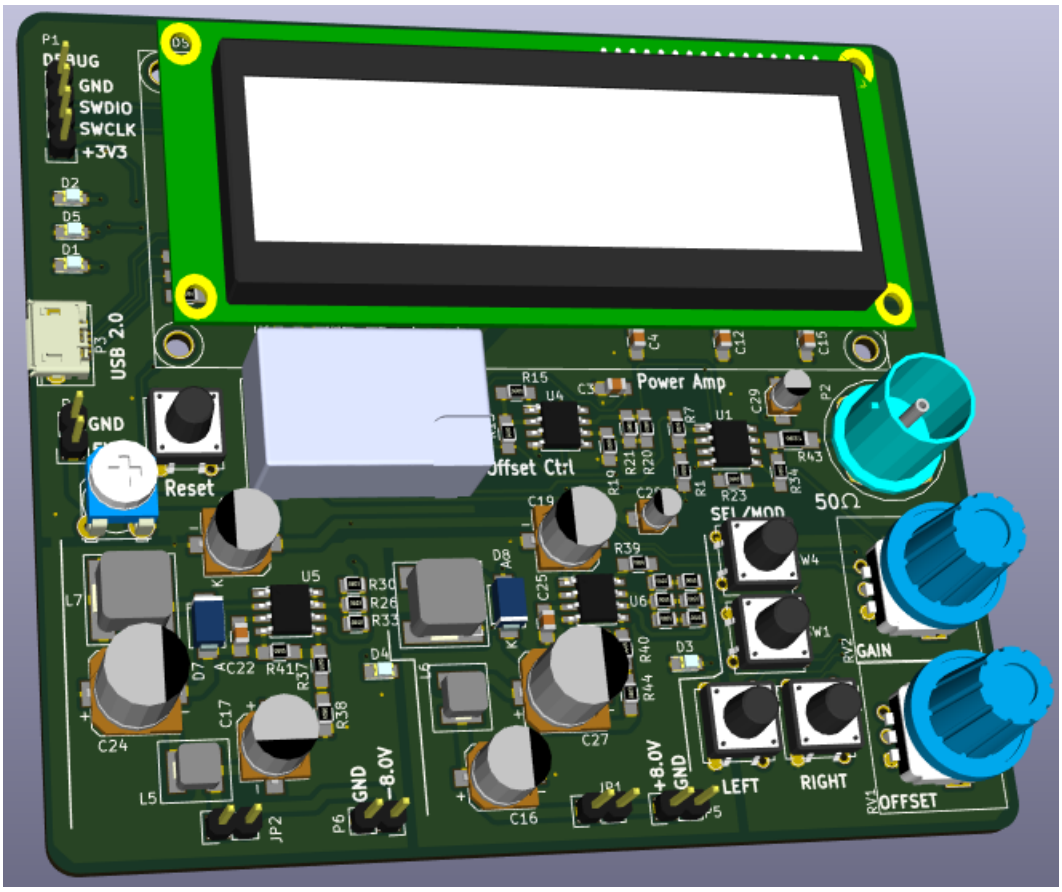


Figure 6.5: 3D image of device after assembly, rendered in KiCAD

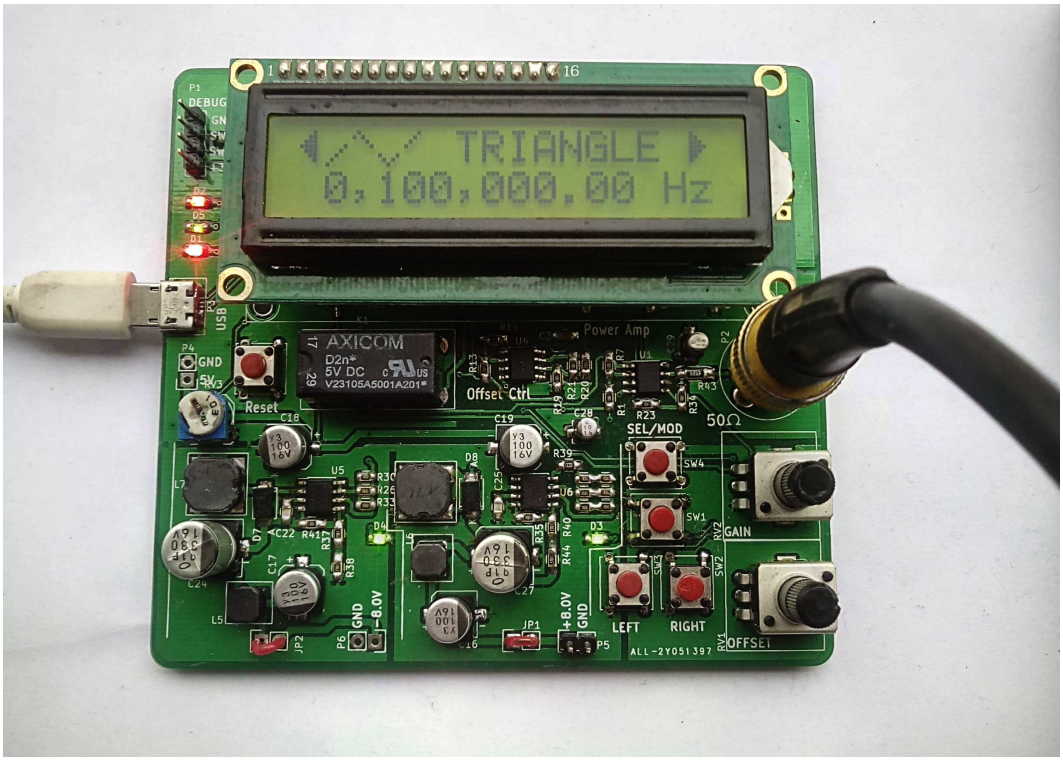


Figure 6.6: Complete device after in-house assembly

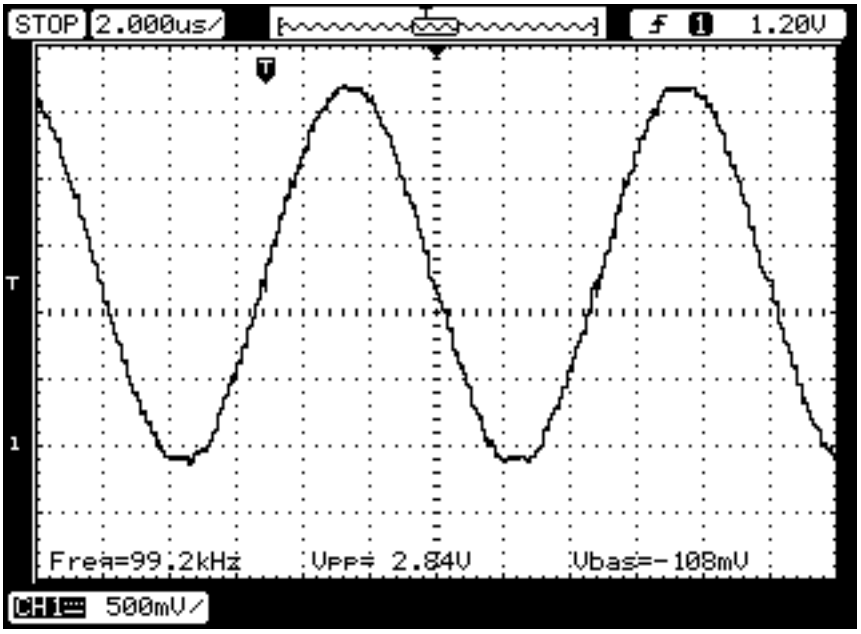


Figure 6.7: Sine Wave generated from final assembled device

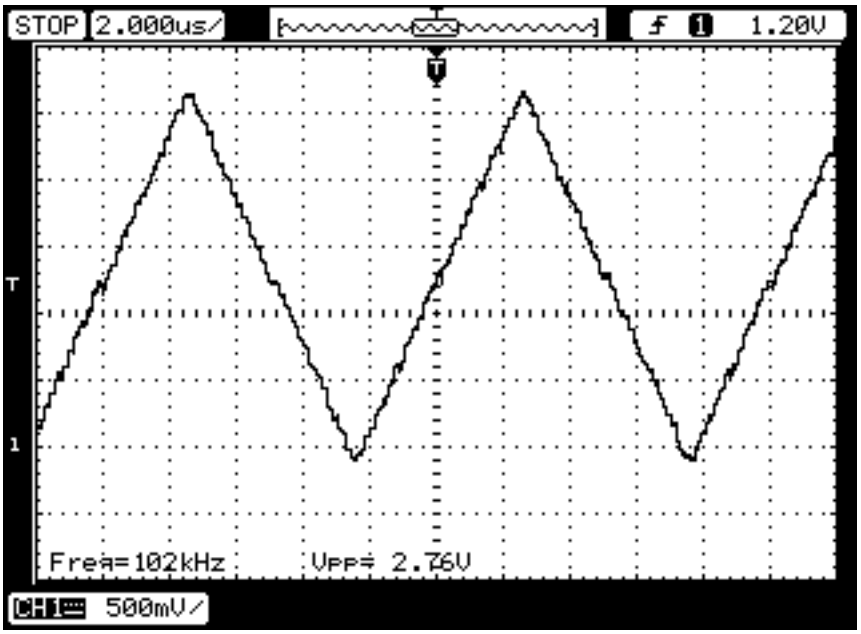


Figure 6.8: Traingle Wave generated from final assembled device

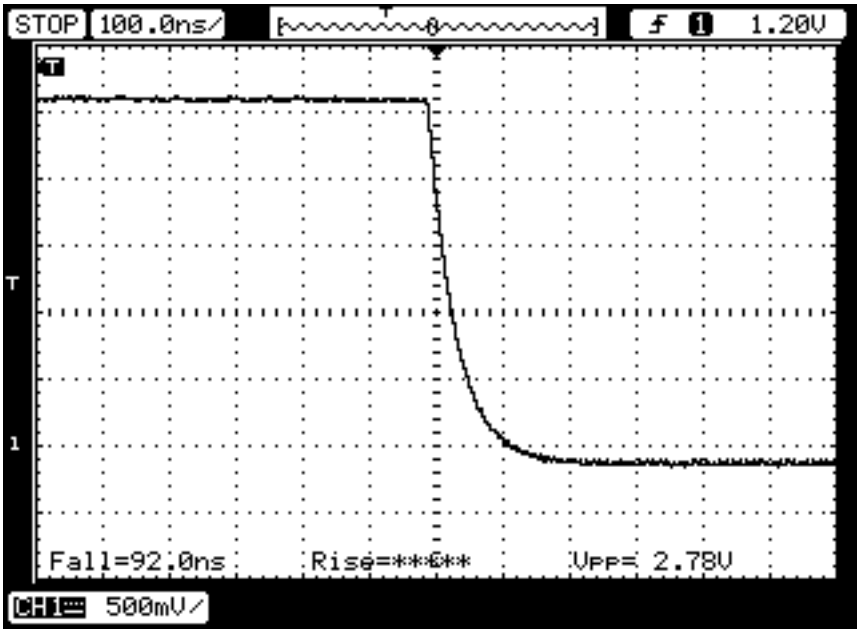


Figure 6.9: Fall time measurement in Rectangular wave
Fall time = 92.0 ns

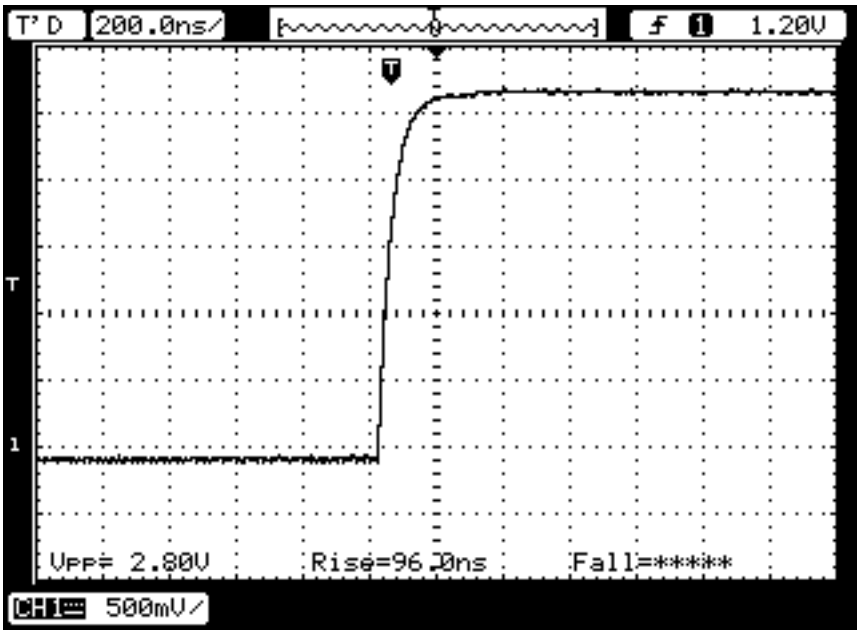


Figure 6.10: Rise time measurement in Rectangular wave
Rise time = 96.0 ns

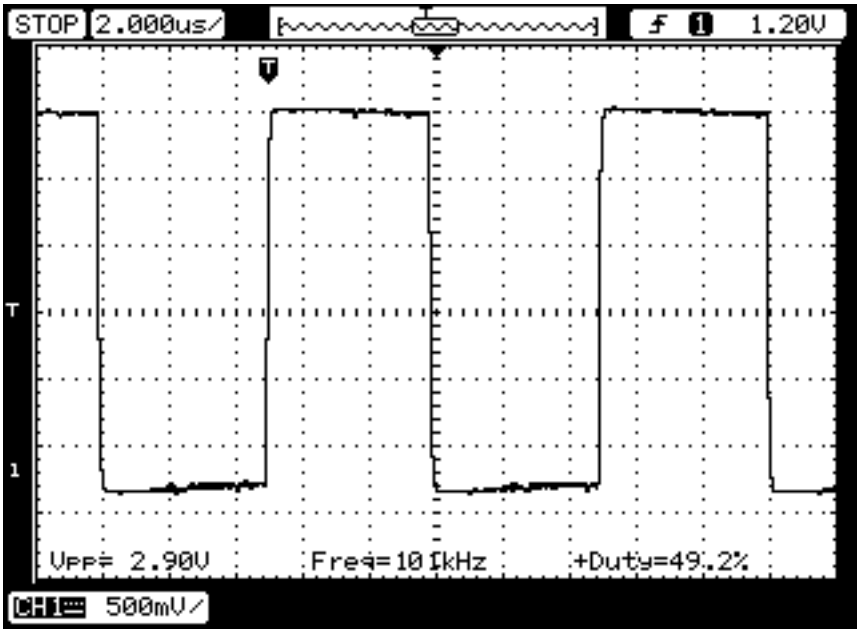


Figure 6.11: Square Wave generated from final assembled device

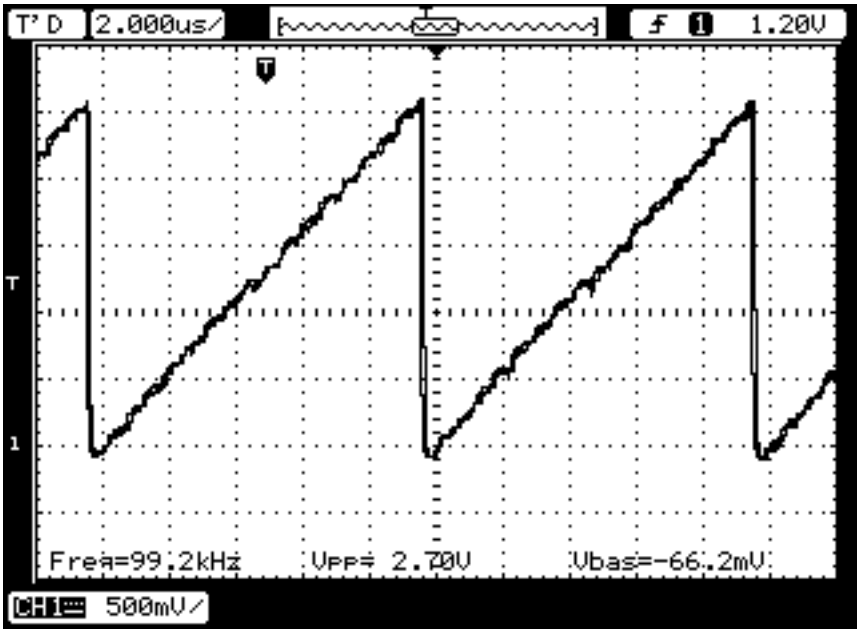


Figure 6.12: Sawtooth Wave generated from final assembled device

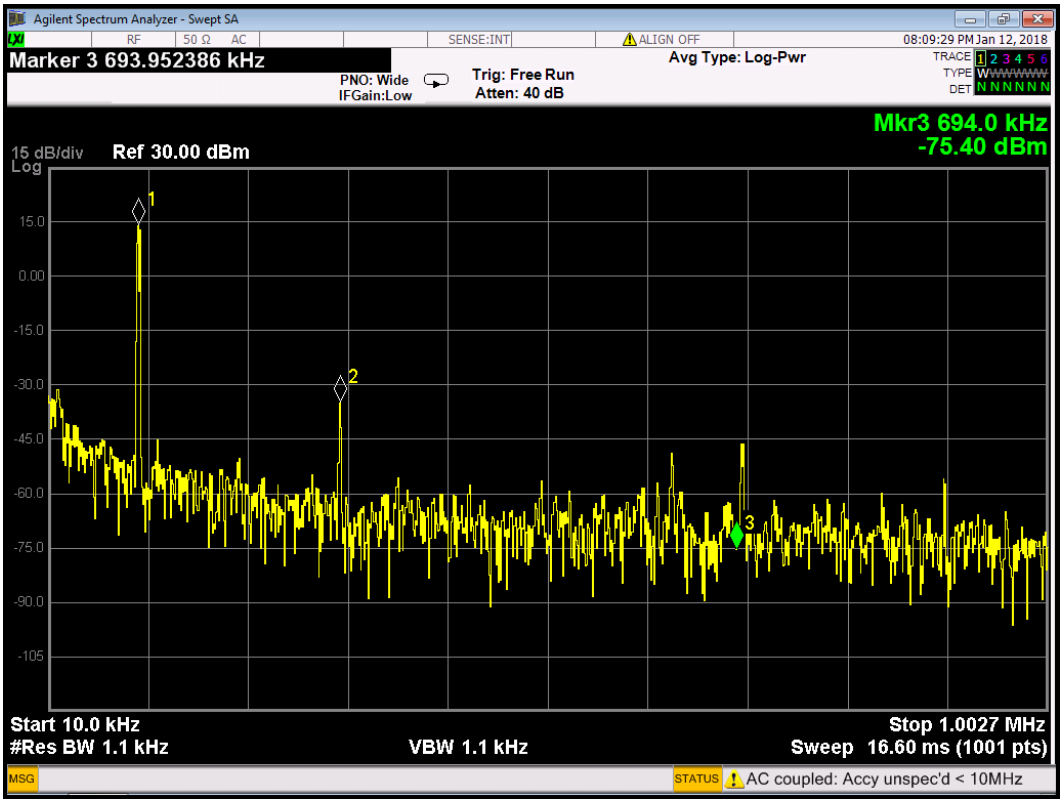


Figure 6.13: Spectral measurements using Agilent PXA Signal Analyser N9030A
SFDR = -50dB, Sine @ 100KHz

Chapter 7

CONCLUSION

7.1 Conclusion

Waveform generators are a fundamental test tool that engineers use for a wide variety of Medium Frequency & Low frequency including Audio applications. This can be used mainly in the developing and testing of electronic hardware. Typical applications are but not limited to:

1. To test and characterize the electronic device and circuit.
2. To create large array of periodic signal source.
3. Information carriers for communication system.
4. Control systems and time clock for computers.

7.2 Limitations

This project is designed basically for academic purposes & day to day test and measurement applications. It is very useful for audio applications as it covers the entire audio spectrum gracefully.

- This design uses operational amplifiers having fixed slew rate which cannot be controlled dynamically so it may cause problems in circuits having higher susceptibility to ringing effects.
- Output load driving capability (which arise due to use of cost sensitive components) it may not be used in applications like antenna driving.
- The Output Impedance is fixed hence it may not match with every load during transmission line application. Higher frequency ($\geq 1MHz$) requirements may not be fulfilled by this design.

7.3 Future Scope

The device after assembly would be having a size of 99.3 mm x 91 mm. It can be compressed further so that it can be integrated as a module in other applications including portable electronics. Some features can be enhanced like the vertical resolution & memory depth by using more expensive microcontroller. The output voltage range is targeted to be increased to upto 20Vpp using external power adapter. Frequency range can be increased using microcontrollers like TM4C129 series (Texas Instruments), STM32F4 series (STMicroelectronics), LPC4300 series (NXP).

Abbreviations

AHB Advanced High-performance Bus. 6

AMBA Advanced Microcontroller Bus Architecture. vii, 6

APB Advanced Peripheral Bus. 6

ARM Advanced RISC Machines. vii, 6, 10, 11, 35

ASIC Application Specific Integrated Circuit. 1

BJT Bipolar Junction Transistor. 35

BNC Bayonet Neill-Concelman. 15

CPLD Complex Programmable Logic Devices. 1

DAC Digital to Analog Converters. 15, 16, 19

DDS Direct Digital Synthesis. iv, 16

DMA Direct Memory Access. 6

DPDT Double Pole Double Throw. 15

DRAM Dynamic Random Access Memory. 1

EEPROM Electrically Erasable Programmable Read-Only Memory. 1

EMI Electro-Magnetic Radiation. 29

ESR Effective Series Resistance. 29

FET Field Effect Transistor. 35

FPGA Field Programmable Gate Array. 1

GPIO General Purpose Input-Output. iv, 3, 6

IDE Integrated Development Environment. vii, 35

MCU Micro-Controller-Unit. iv, vii, 1, 2, 6, 11, 35

MOS Metal Oxide Semiconductor. 35

NVIC Nested Vectored Interrupt Controller. 1, 6

OEM Original Equipment Manufacturers. 1

PCB Printed Circuit Board. 35

SFR Special Function Registers. 35

SPICE Simulation Program with Integrated Circuit Emphasis. 35

SRAM Static Random Access Memory. iv, 1, 6, 11, 16

SWD Serial Wire Debug. 35

USB Universal Serial Bus. iv, 26

References

[1] Jade Alberkrack. “Theory and Applications of the MC34063 and˜ A78S4O Switching Regulator Control Circuits”. In: *Application Note AN920, Motorola Semiconductor Product Sector, Tempe, AZ* (1989).

[2] Lionel Cordesses. “Direct digital synthesis: A tool for periodic wave generation (part 1)”. In: *IEEE Signal processing magazine* 21.4 (2004), pp. 50–54.

[3] Kai Hwang and A Faye. “Computer architecture and parallel processing”. In: (1984).

[4] Alan V Oppenheim. *Discrete-time signal processing*. Pearson Education India, 1999.

[5] John G Proakis and Dimitris G Manolakis. *Digital signal processing 3 rd edition*. 1996.

[6] Mahmoud Harmouch Shafi Sekander. *Application of the MC34063 Switching Regulator*. 1st ed. Texas Instruments. Sept. 2006.

[7] Steven W Smith et al. “The scientist and engineer’s guide to digital signal processing”. In: (1997).

[8] Ikuo Yasui and Yukihiko Shimazu. *Microprocessor with harvard architecture*. US Patent 5,034,887. July 1991.

[9] Joseph Yiu. *The definitive guide to the ARM Cortex-M3*. Newnes, 2009.