Synchronous Switching Buck Regulator

Final Project (Jul-Nov 2018)

EE5325-Power Management Integrated Circuits

Subha Sarkar
Rupam K Chakraborty

Department of Electrical Engineering
Indian Institute of Technology, Madras

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Introduction

Synchronous Switching DC-DC buck converter

Why switching ? Most of the switching regulators have lossless components which does not dissipate power so efficiency is better than linear counterpart.

Why Synchronous ? It almost eliminates the flyback-diode power loss (found in non-synchronous) by putting a low resistance path (NMOS) in parallel with the diode. The driver circuit now becomes complex (Dead time control).

What is buck ? It is topology in which output voltage is always lesser than the input voltage.

Topology

Voltage mode feed-forward topology [7]

Advantages

1. Simplicity (Compensator design maybe complex)
2. Devoid of dual feedback network (found in CMC)
3. No requirement of slope compensation
4. Supports high Dynamic range of output load current.

Disadvantages

1. Slow line regulation (Solved using Feed-forward topology [6]).

Component Selection

Inductor Selection

For reduced RMS Loss, the inductor ripple is chosen to be 10% of Average(load) current (1A). So inductor ripple is chosen to be 100mA.

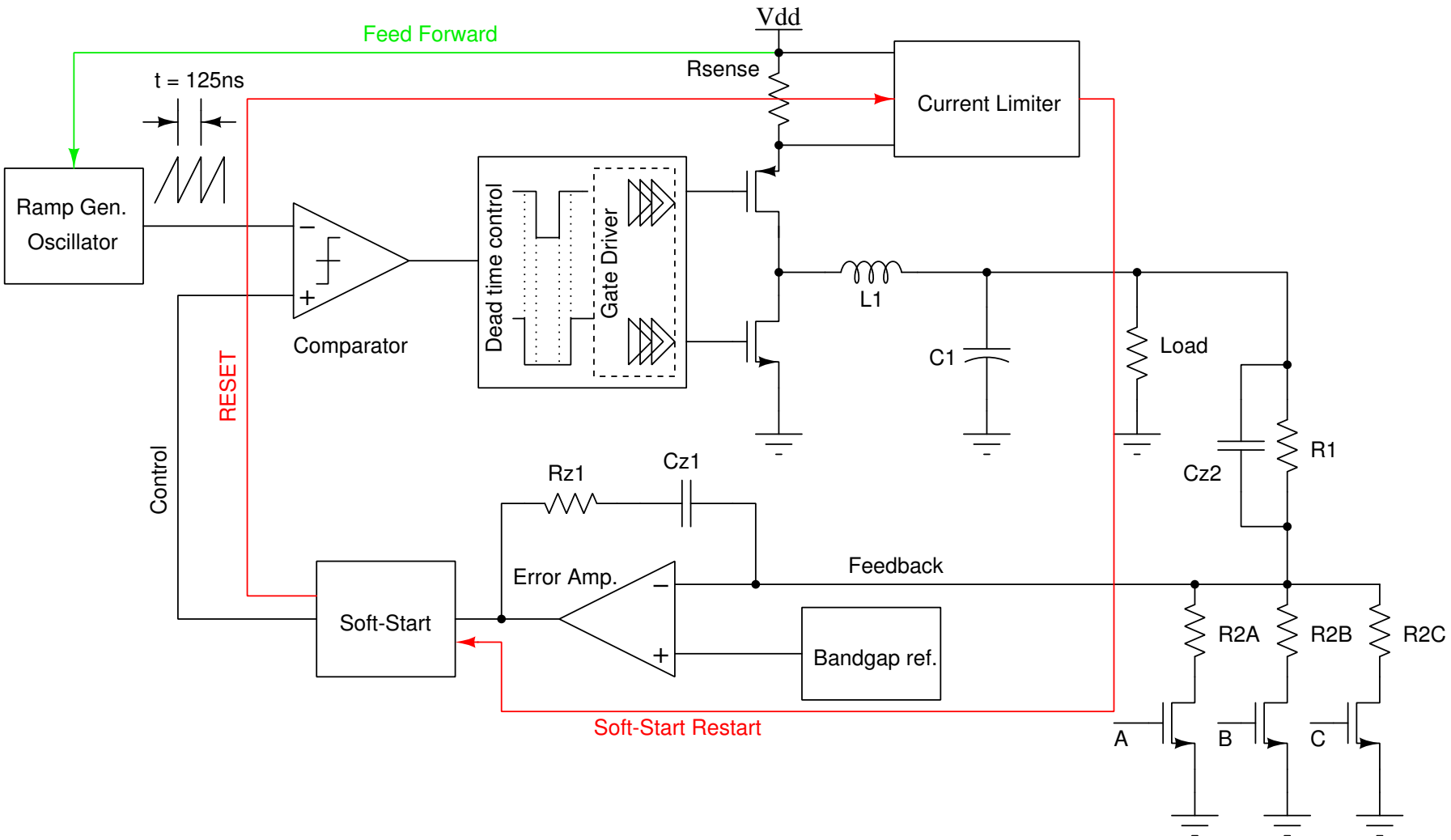
$$L = \frac{V_{in}.D.(1-D)}{\Delta I.F_{sw}} \implies L = 0.5625uH \tag{1}$$

Capacitor Selection

To get minimum ripple we used following relation,

$$C = \frac{V_{in}.D.(1-D)}{8.L.\Delta V.F_{sw}^2} \tag{2}$$

Architecture



Power MOSFET sizing I

Given,

$$\eta = 90\% \tag{3}$$
$$R_{dcr} = 32m\Omega \ (L = 0.47uH) \tag{4}$$
$$R_{sense} = 10m\Omega \tag{5}$$
$$P_{out}(for\ worst\ case) = 0.8W \ (V_{out} = 0.8V) \tag{6}$$
$$I_{load}(max.) = 1A \tag{7}$$
$$\mu.C_{ox}/2 = 175.4uA/V^2, -35.6uA/V^2 \tag{8}$$

Assumptions

Switching loss = 0.3×Conduction Loss at 1A [9]
$R_{PMOS} = R_{NMOS} = R_{ds}$

Power MOSFET sizing II

Therefore Conduction loss, $P_{conduction}$

$$P_{conduction} = I_{load}^2.(R_{dcr} + R_{ds} + R_{sense}) = \left(\frac{1}{\eta} - 1\right).\frac{P_{out}}{1.3} \quad (9)$$

$$\implies R_{ds} = 68.37m\Omega - 32m\Omega - 10m\Omega = 26.37m\Omega \quad (10)$$

$$\left(\frac{W}{L}\right) = \frac{1}{\mu.C_{ox}.(V_{gs} - V_t).R_{MOS}} \quad (11)$$

$$\implies \left(\frac{W}{L}\right)_n = 83799 \implies W_n = 15.08mm \quad (12)$$

$$\implies \left(\frac{W}{L}\right)_p = 412876 \implies W_p = 74.33mm \quad (13)$$

Comparator

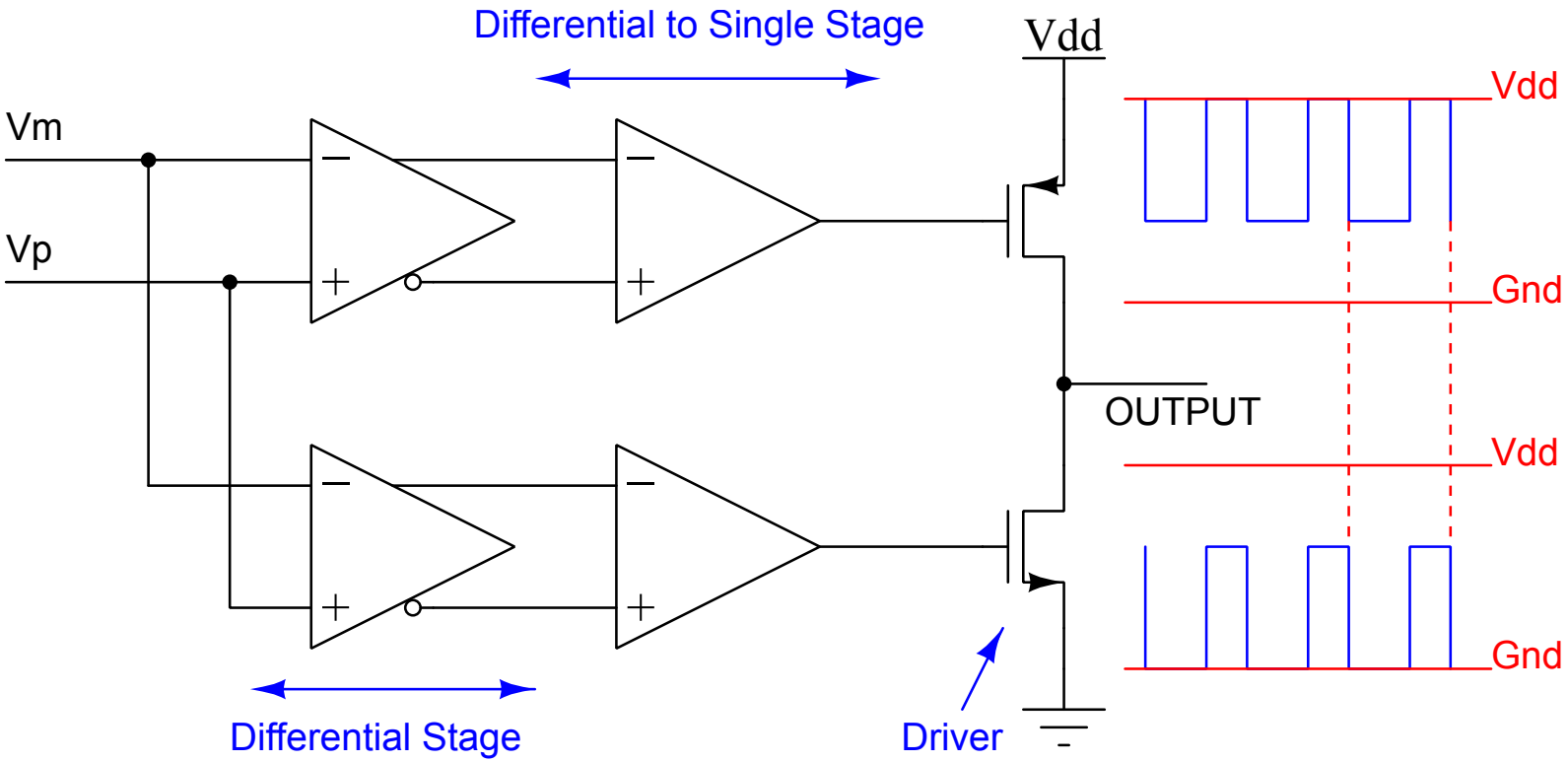


Figure: Comparator block diagram [5]

Oscillator & Ramp Generator

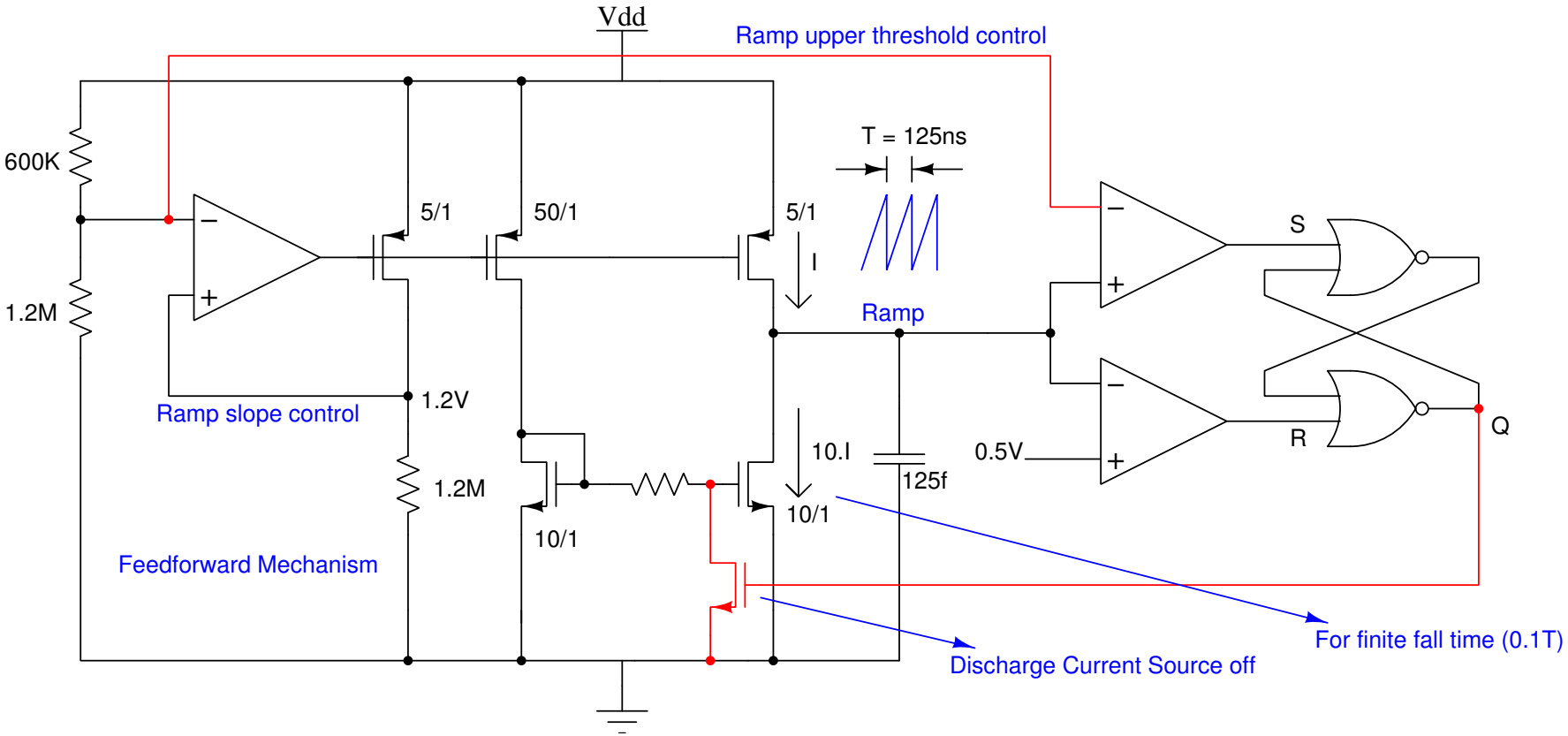


Figure: Oscillator & Ramp Generator[3]

Soft Start

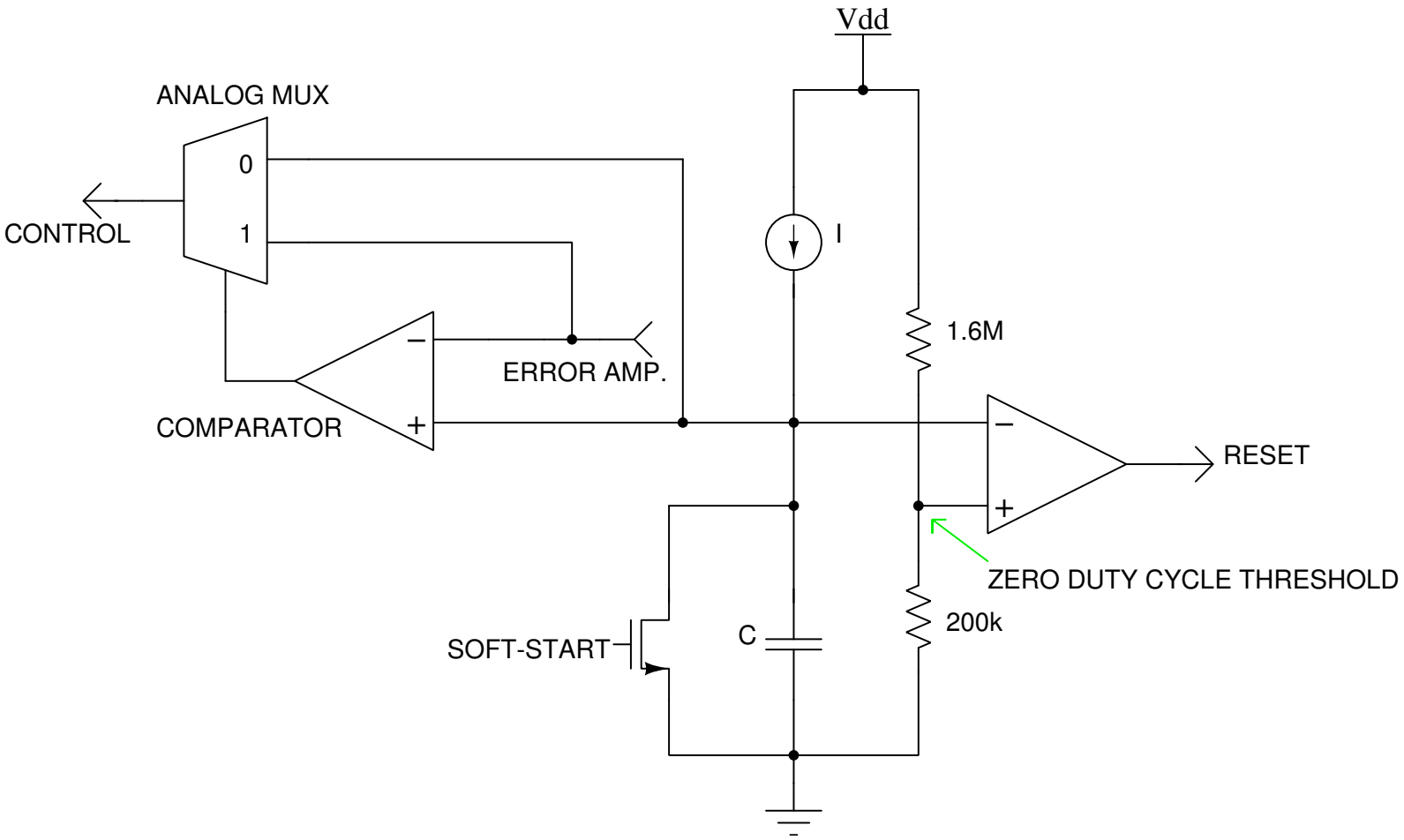


Figure: Soft Start

Current Limiter

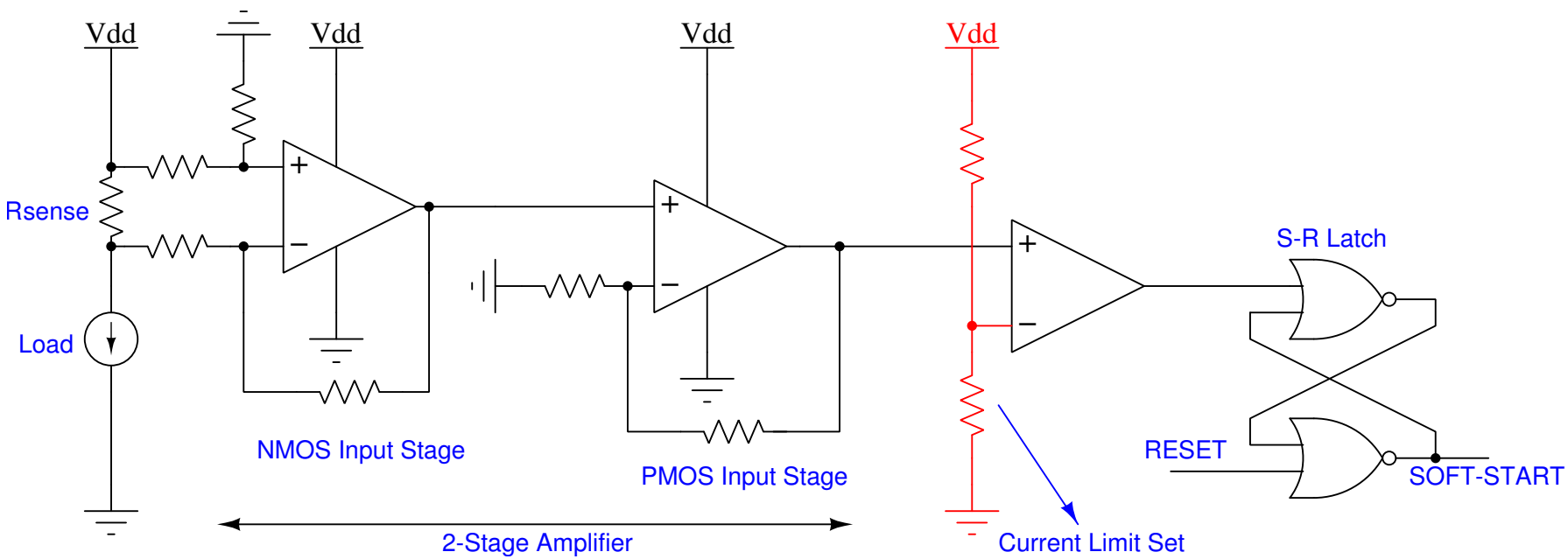


Figure: High Side Current Sensor[11][4] and Short circuit limiter with Auto-Wake up (Hicup) Mode

Bandgap Reference

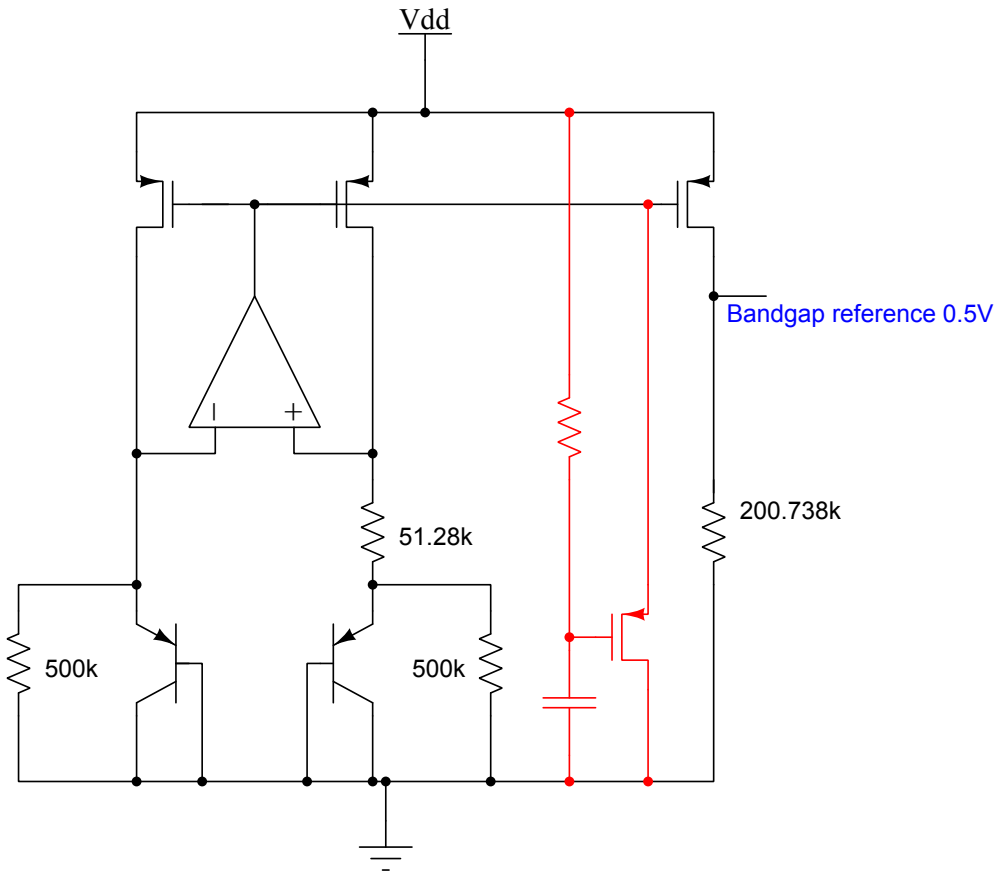


Figure: Current mode Sub-1V bandgap reference[1]

Amplifier

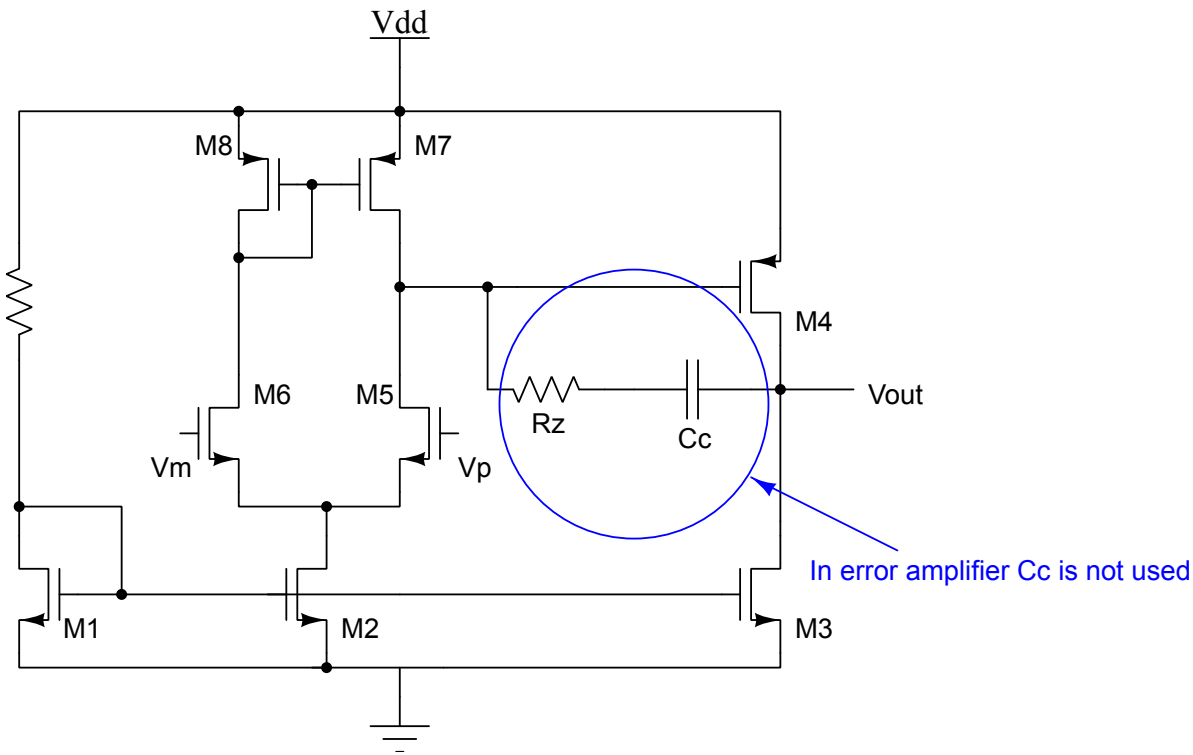


Figure: Schematic of Amplifiers used.

Dead time generator & Gate drivers

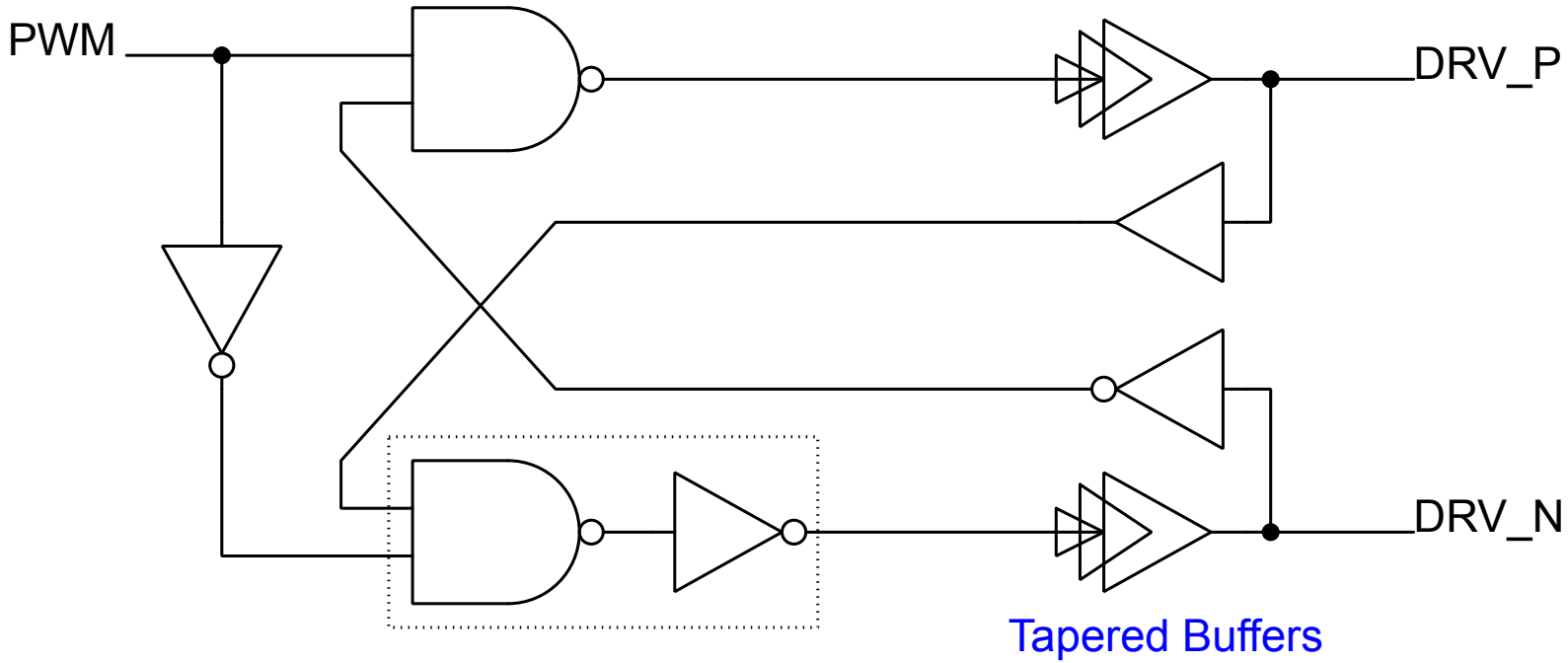


Figure: Gate drivers[2] and Dead time generator; Scaling factor of tapered buffers = 6 and No. of stages = 4

Novelty

1. **Softstart circuit [8] [10]** - It limits Inrush Current along with Duty cycle continuity which reduces the peaking.
2. **Peak Current Limit** - It restarts the soft-start cycle to slowly increase the output voltage & checks if the short still exists or not. High side sensing [11] is implemented for this purpose.
3. **Startup circuit of Bandgap reference [1]** - A RC Circuit based Startup Circuit which consumes no current at steady state.
4. **Oscillator & Feedforward** - It improves the line regulation speed [7] in voltage mode control.

General Results

Parameters	**Values**
Input voltage Range	1.7 - 1.8V
Output Range	0.5 - 1.6V
Load Current Range	1mA-1A
Switching Frequency	7.98MHz
Inductor	0.47u
Capacitor	11u

Table: General Results for all upcoming slides

Bandgap Reference

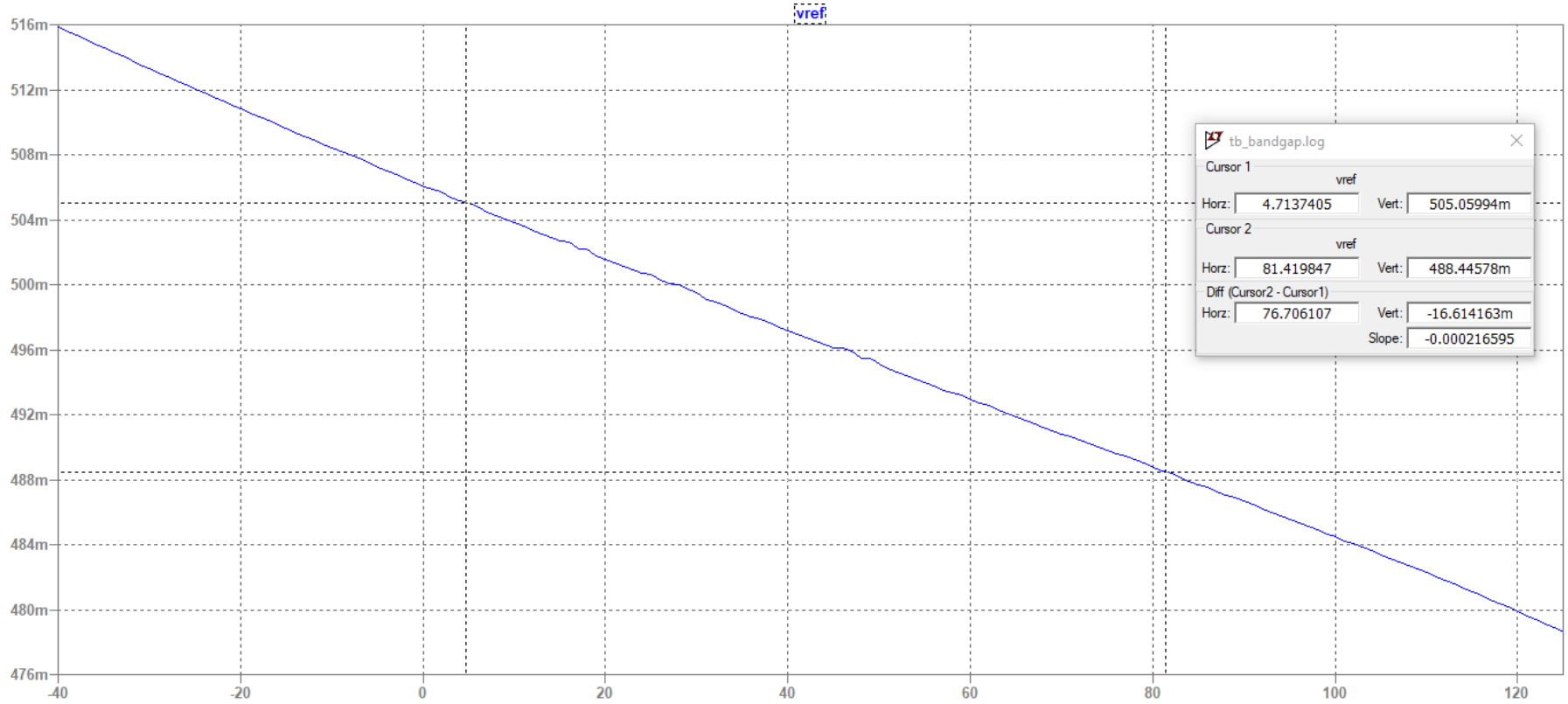


Figure: Bandgap reference temperature curve

Compensator

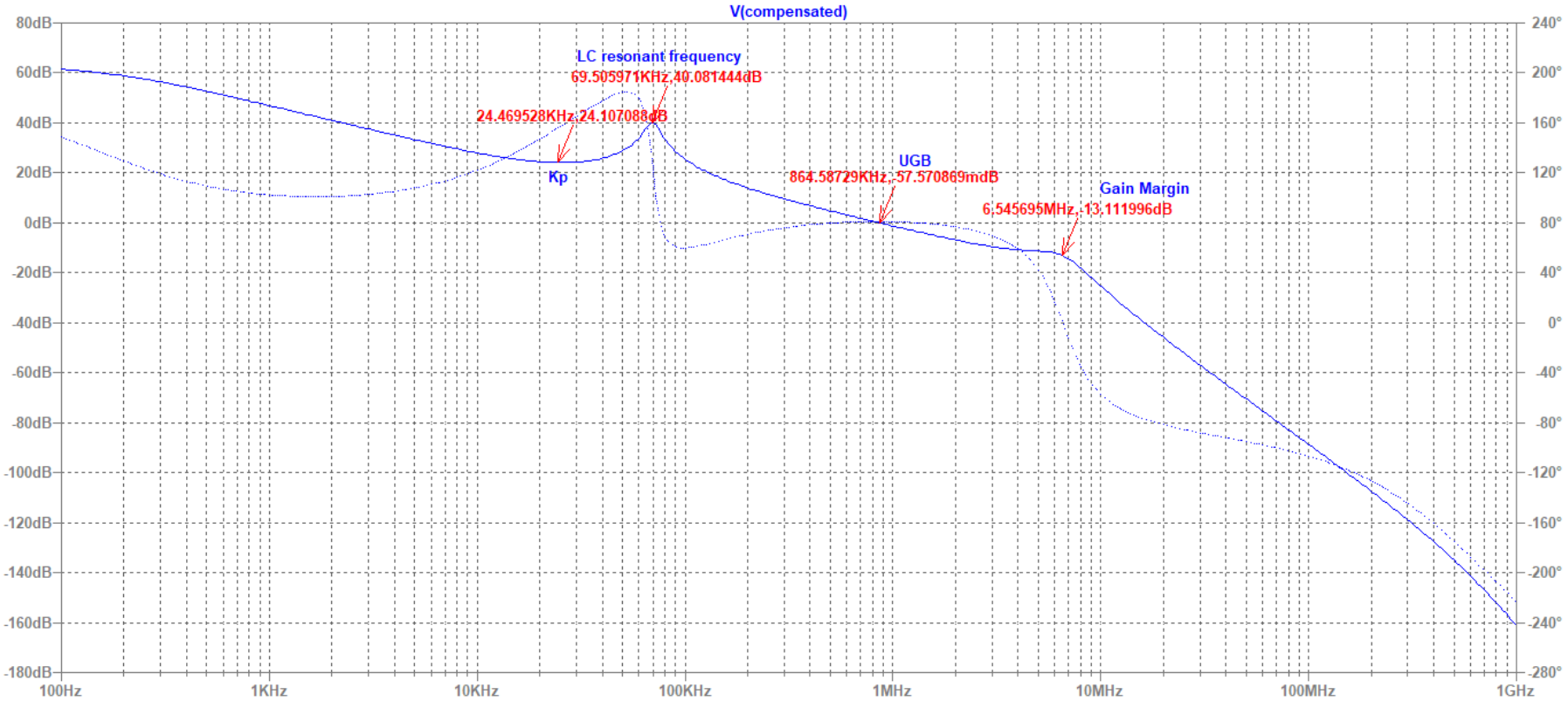


Figure: Compensator Frequency response

Simulation Results I

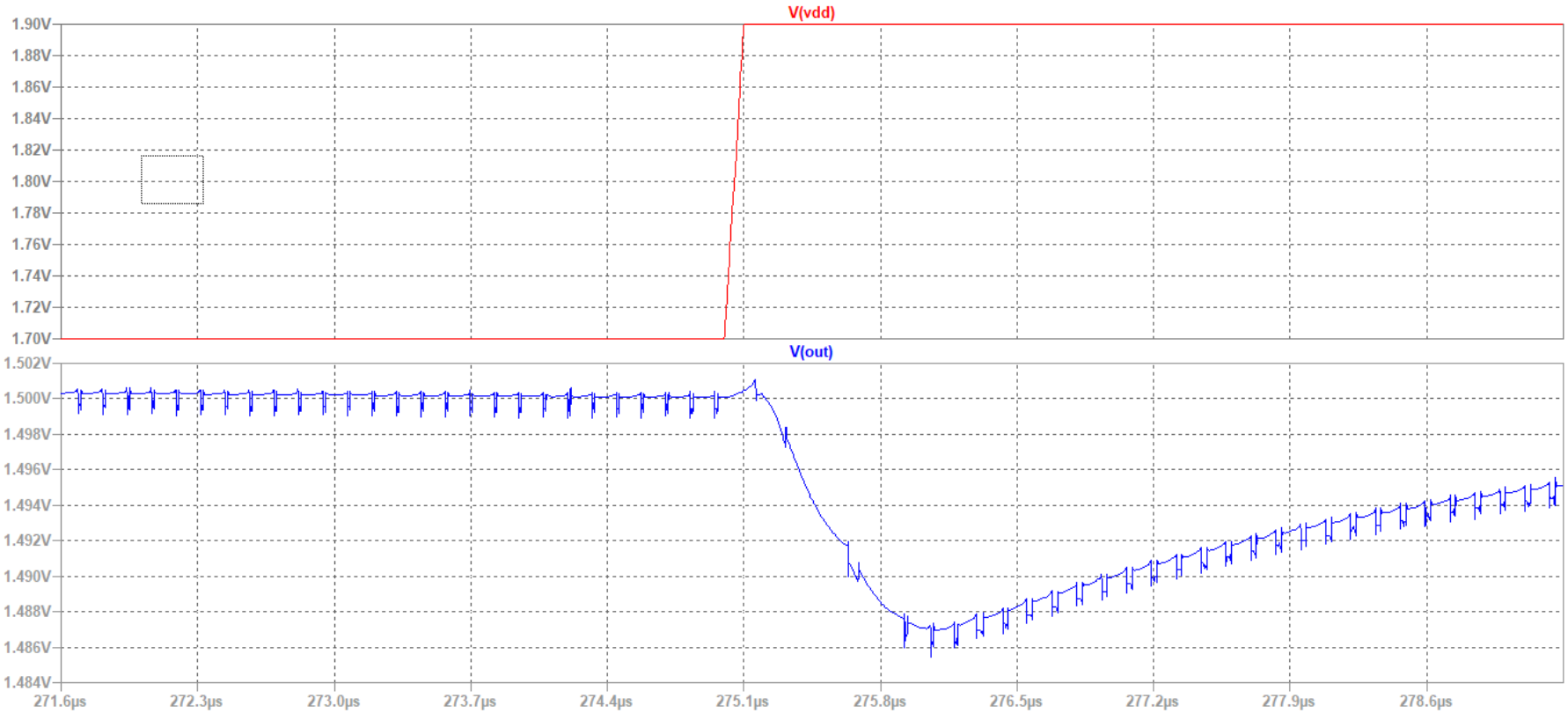


Figure: Line transient for rising VDD, $V_{out} = 1.5V$

Simulation Results II

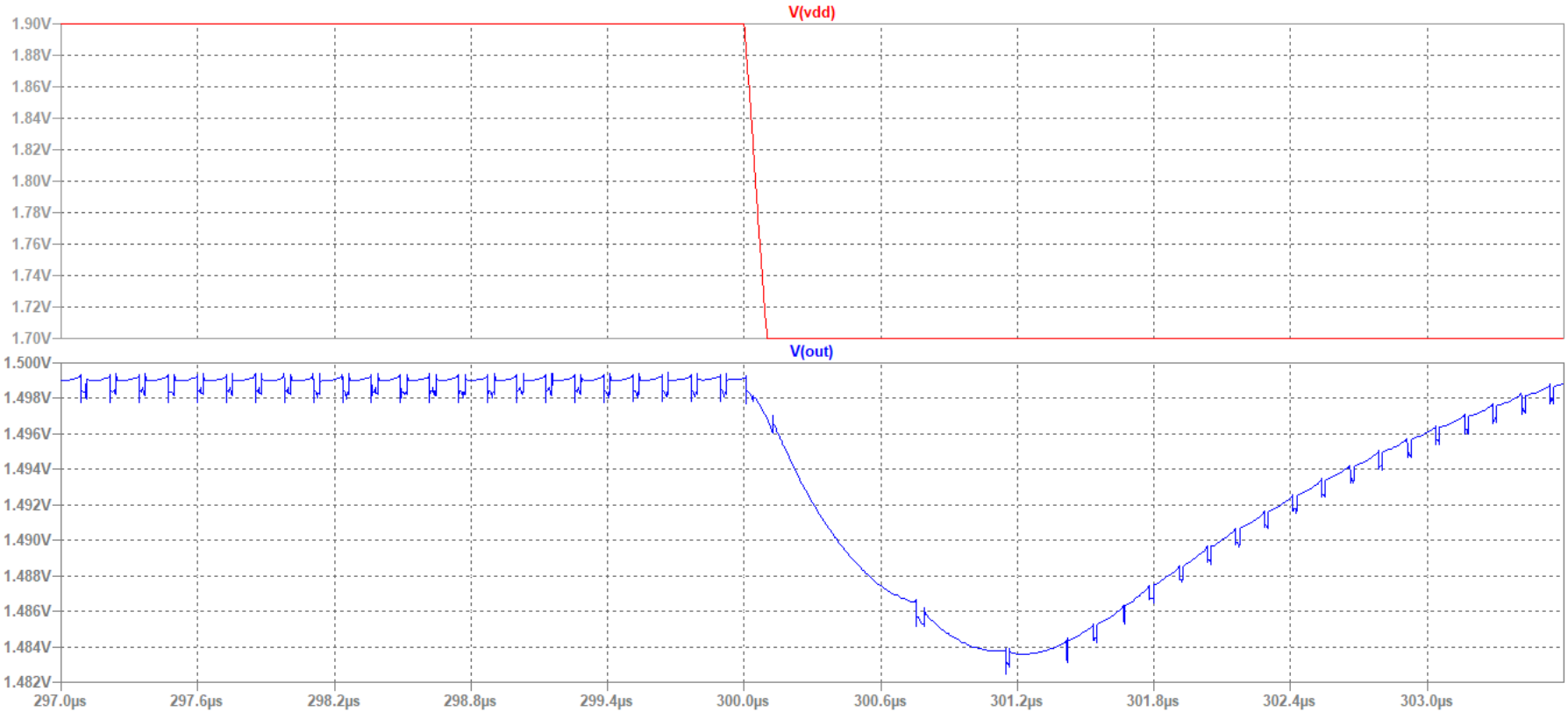


Figure: Line transient for falling VDD, $V_{out} = 1.5V$

Simulation Results III

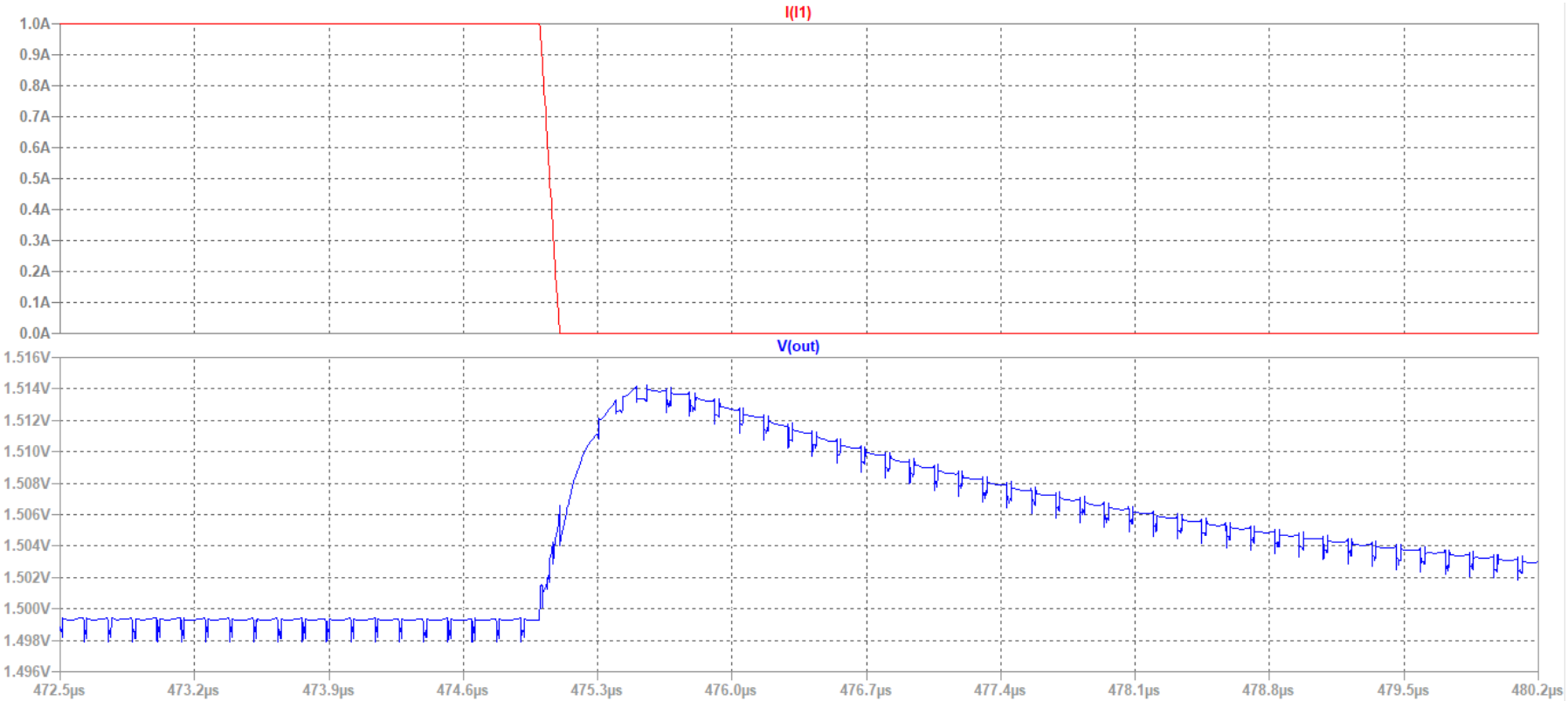


Figure: Load Transient Overshoot response for $V_{out} = 1.5V$

Simulation Results IV

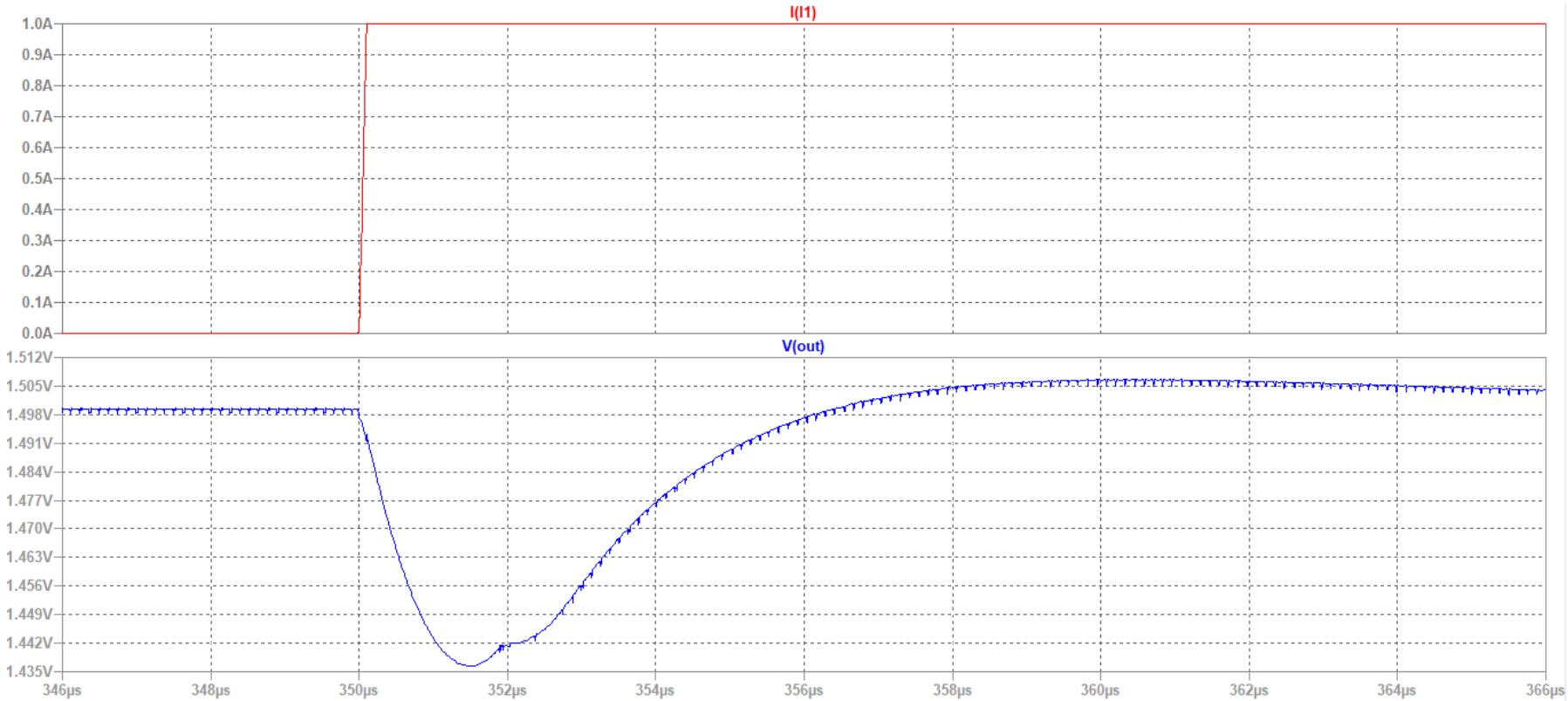


Figure: Load Transient Undershoot response for $V_{out} = 1.5V$

Simulation Results V

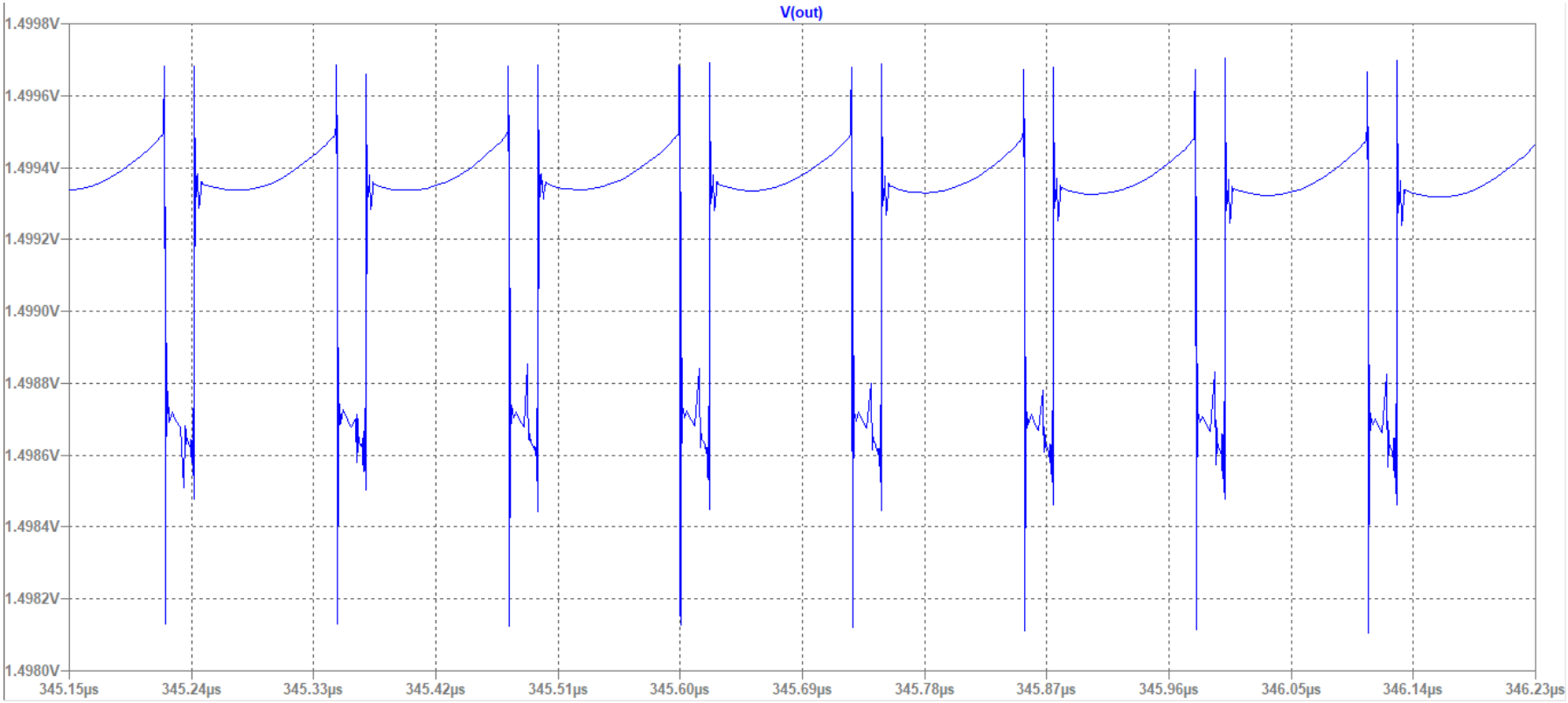


Figure: Output ripple for $V_{out} = 1.5V$

Performance Table - $V_{out} = 1.5V$

Parameters	**Results/Values (1mA)**	**Results/Values (1A)**
Settling time (PWM Cycles)	22	
DC output voltage inaccuracy	0.0533%	0.0333%
Overshoot (Load Transient)	0.988%	
Undershoot (Load Transient)	4.193%	
Overshoot (Line Transient)	0.978%	1.298%
Undershoot (Line Transient)	1.064%	1.113%
Efficiency (%)	13.6%	93.79%
Output ripple voltage (PWM)	1.42mVpp	1.53mVpp
FOM2	1.021×10^{-5}	

Table: Performance parameters for $V_{out} = 1.5V$

Simulation Results I

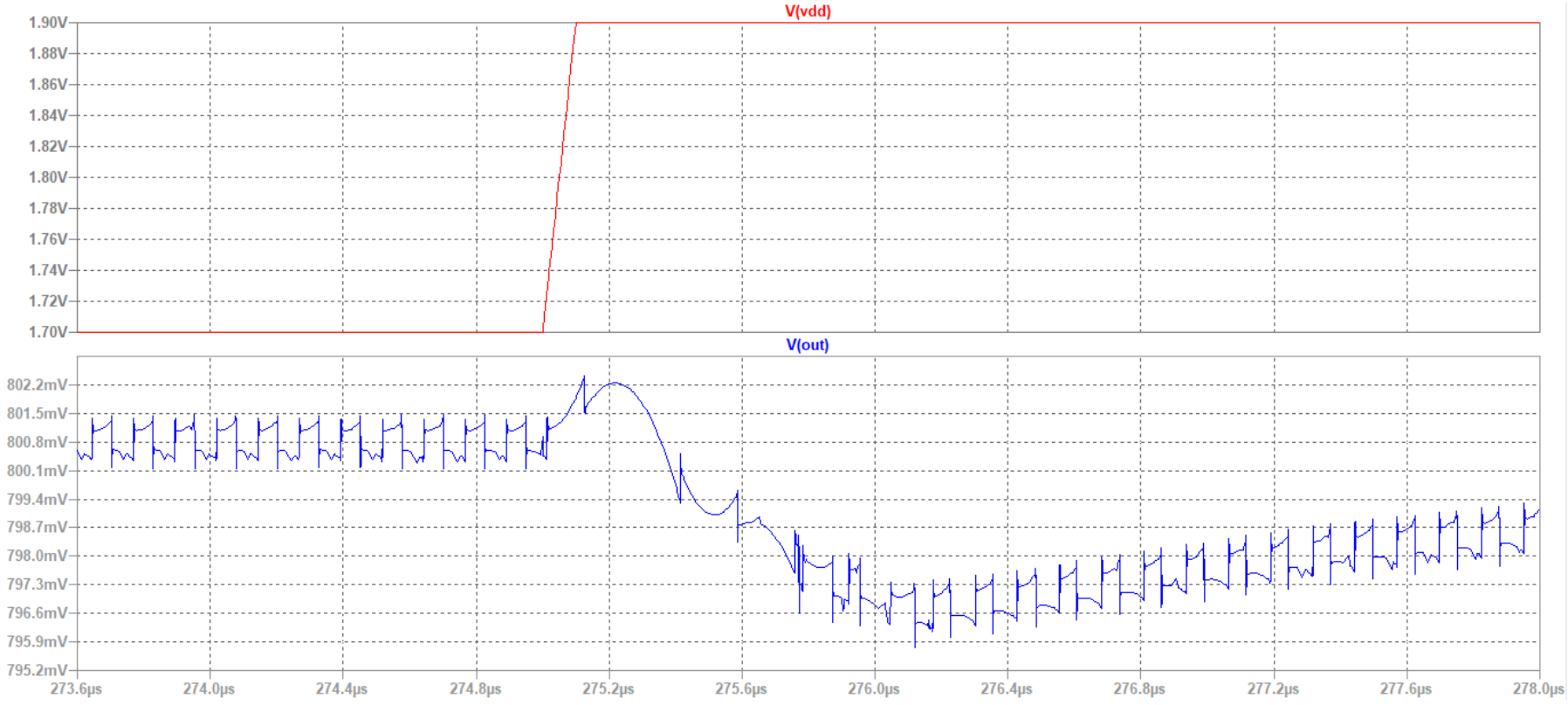


Figure: Line transient for rising VDD, $V_{out} = 0.8V$

Simulation Results II

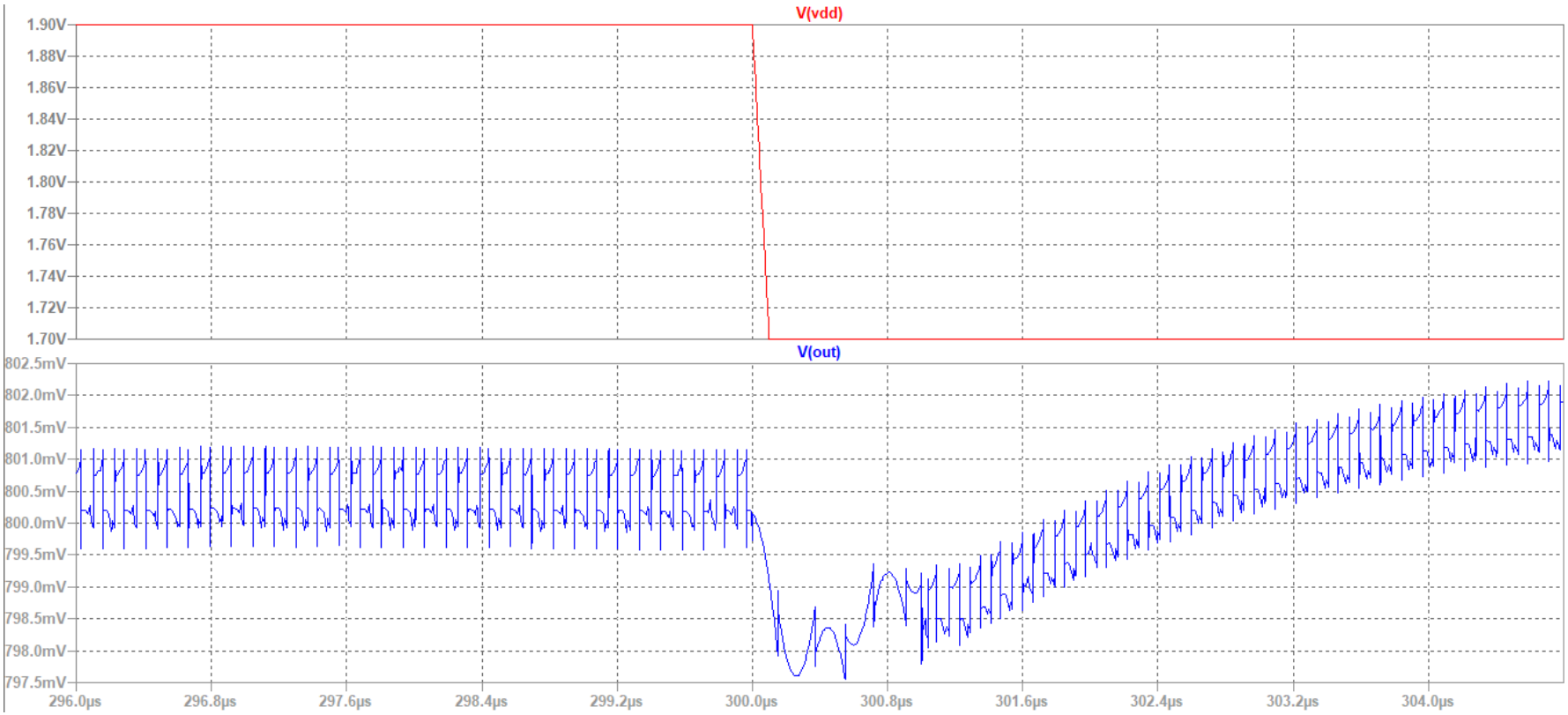


Figure: Line transient for falling VDD, $V_{out} = 0.8V$

Simulation Results III

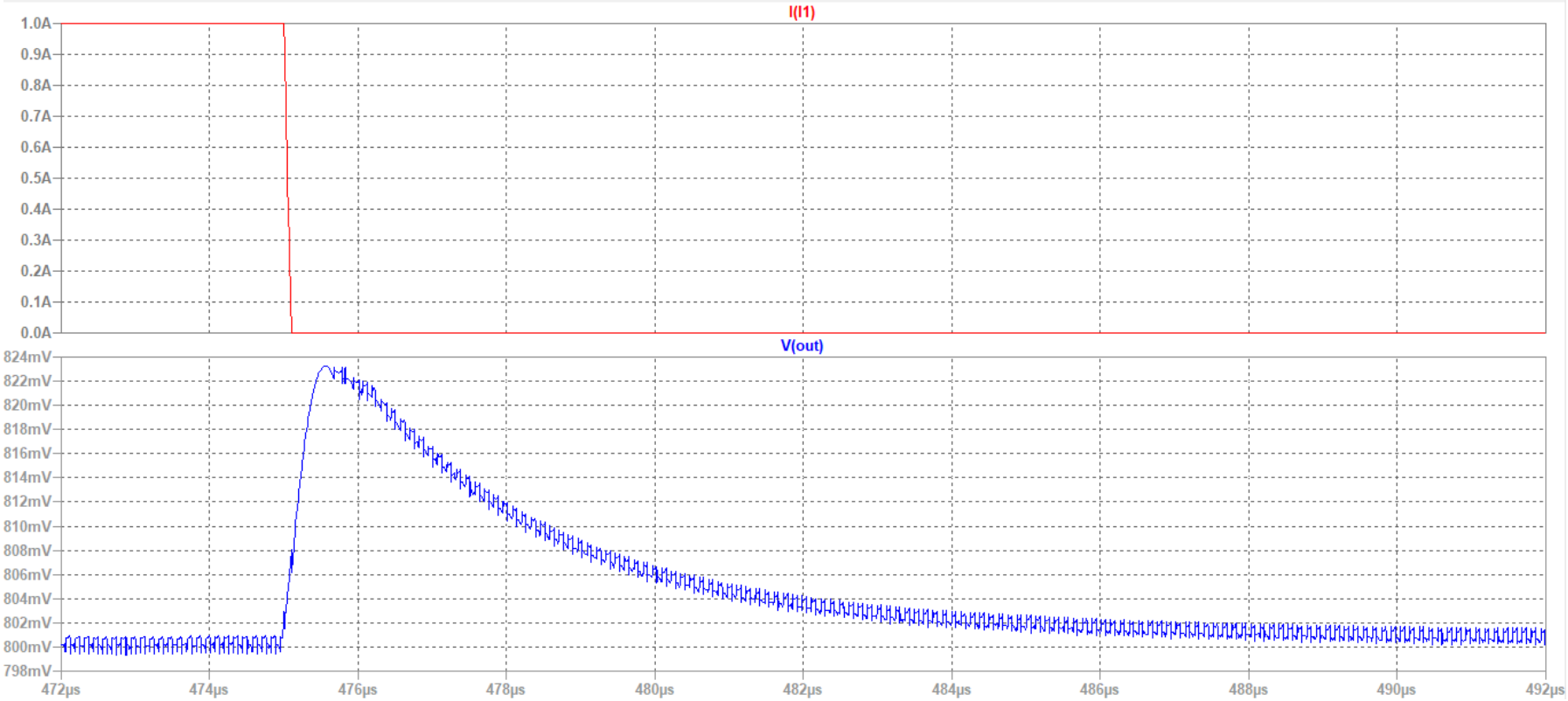


Figure: Load Transient Overshoot response for $V_{out} = 0.8V$

Simulation Results IV

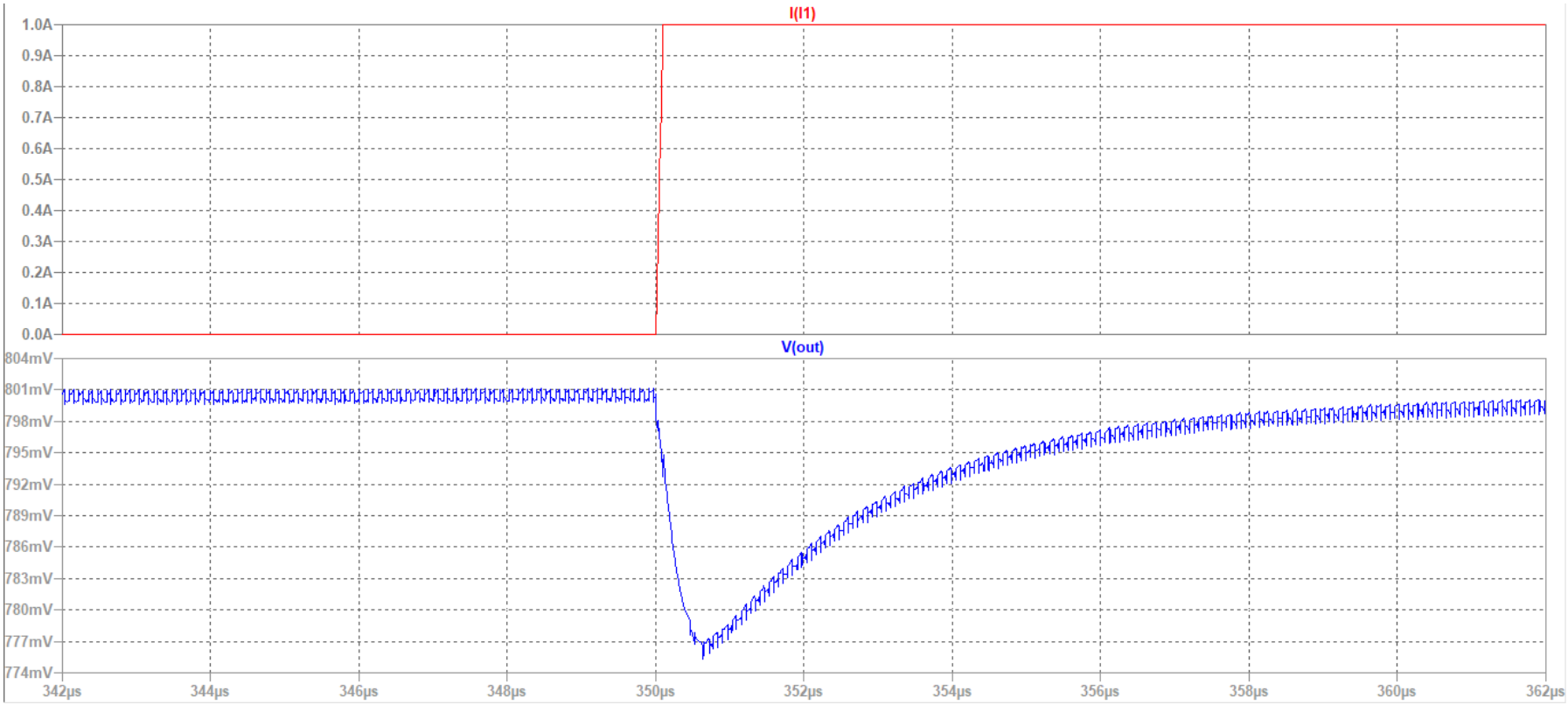


Figure: Load Transient Undershoot response for $V_{out} = 0.8V$

Simulation Results V

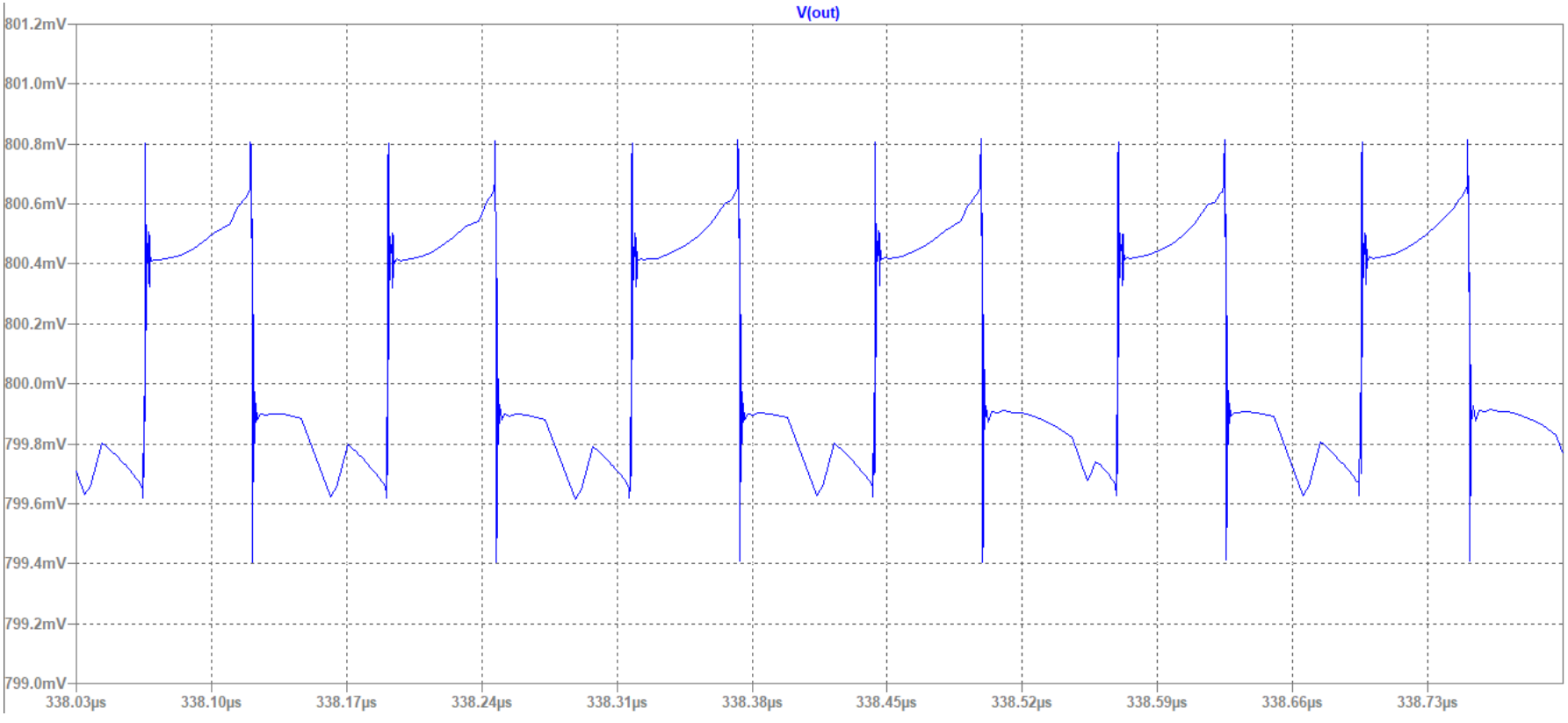


Figure: Output ripple for $V_{out} = 0.8V$

Performance Table - $V_{out} = 0.8V$

Parameters	**Results/Values (1mA)**	**Results/Values (1A)**
Settling time (PWM Cycles)	14	
DC output voltage accuracy	0.016%	0.04%
Overshoot (Load Transient)	2.880%	
Undershoot (Load Transient)	3.036%	
Overshoot (Line Transient)	0.388%	0.151%
Undershoot (Line Transient)	0.145%	0.257%
Efficiency (%)	9.8%	82.61%
Output ripple voltage (PWM)	1.39mVpp	1.53mVpp
FOM2	2.86×10^{-5}	

Table: Performance parameters for $V_{out} = 0.8V$

Simulation Results I

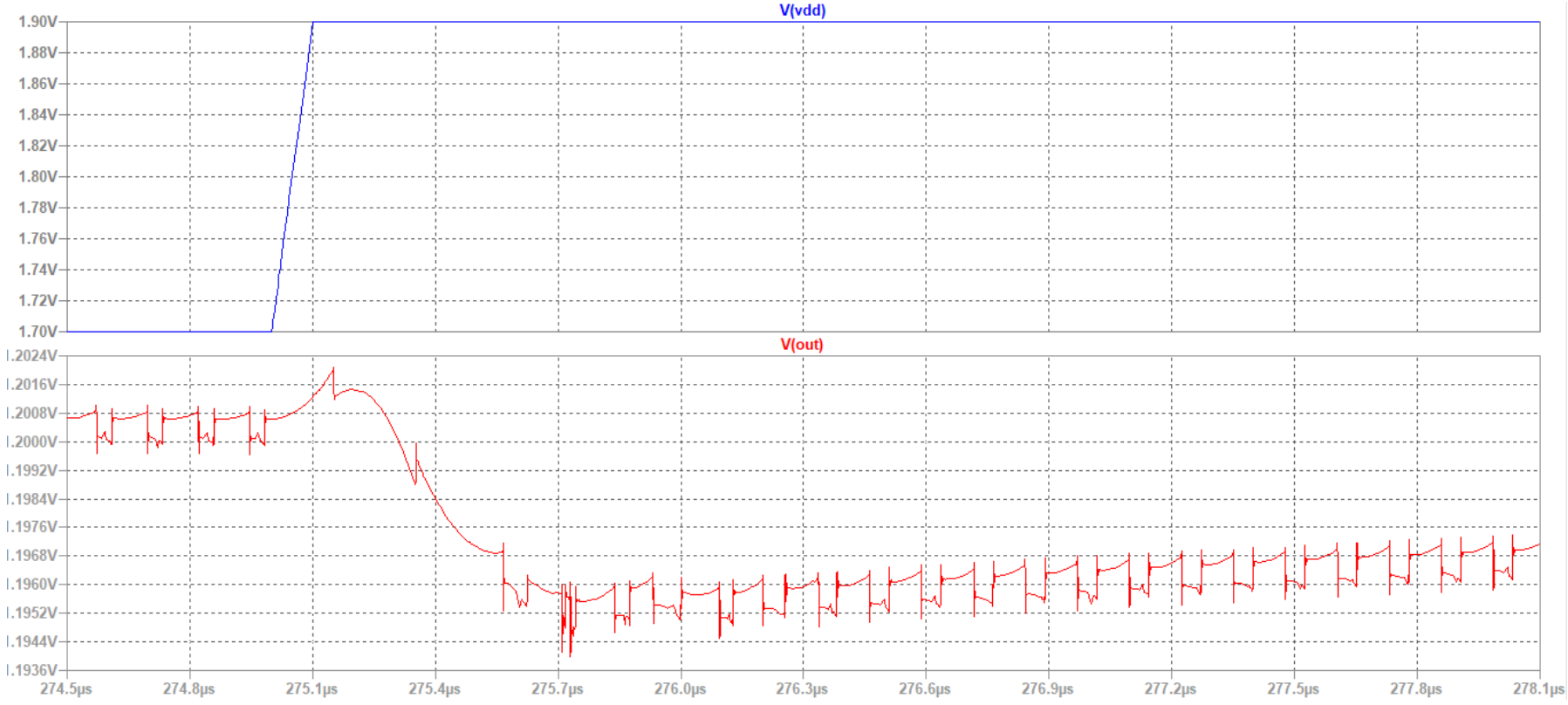


Figure: Line transient for rising VDD, $V_{out} = 1.2V$

Simulation Results II

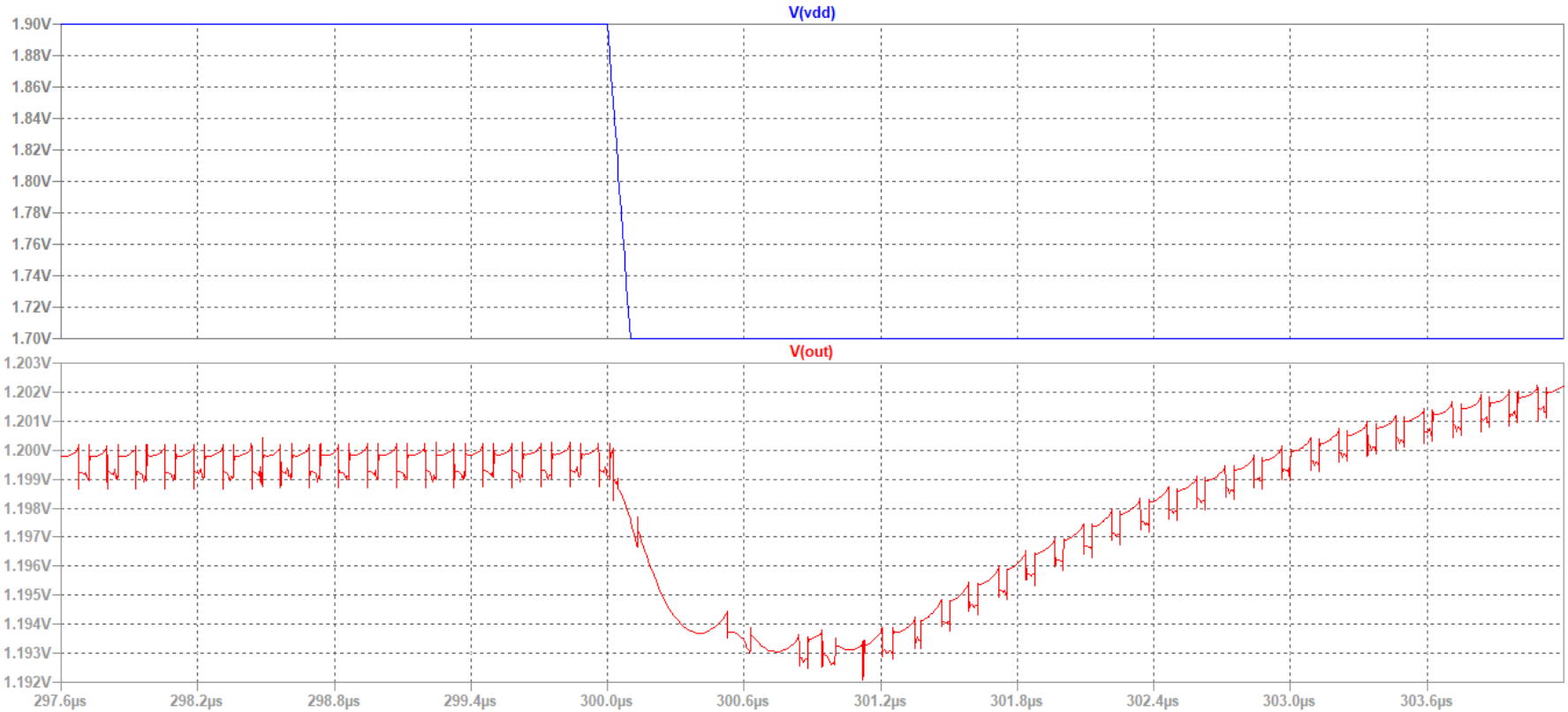


Figure: Line transient for falling VDD, $V_{out} = 1.2V$

Simulation Results III

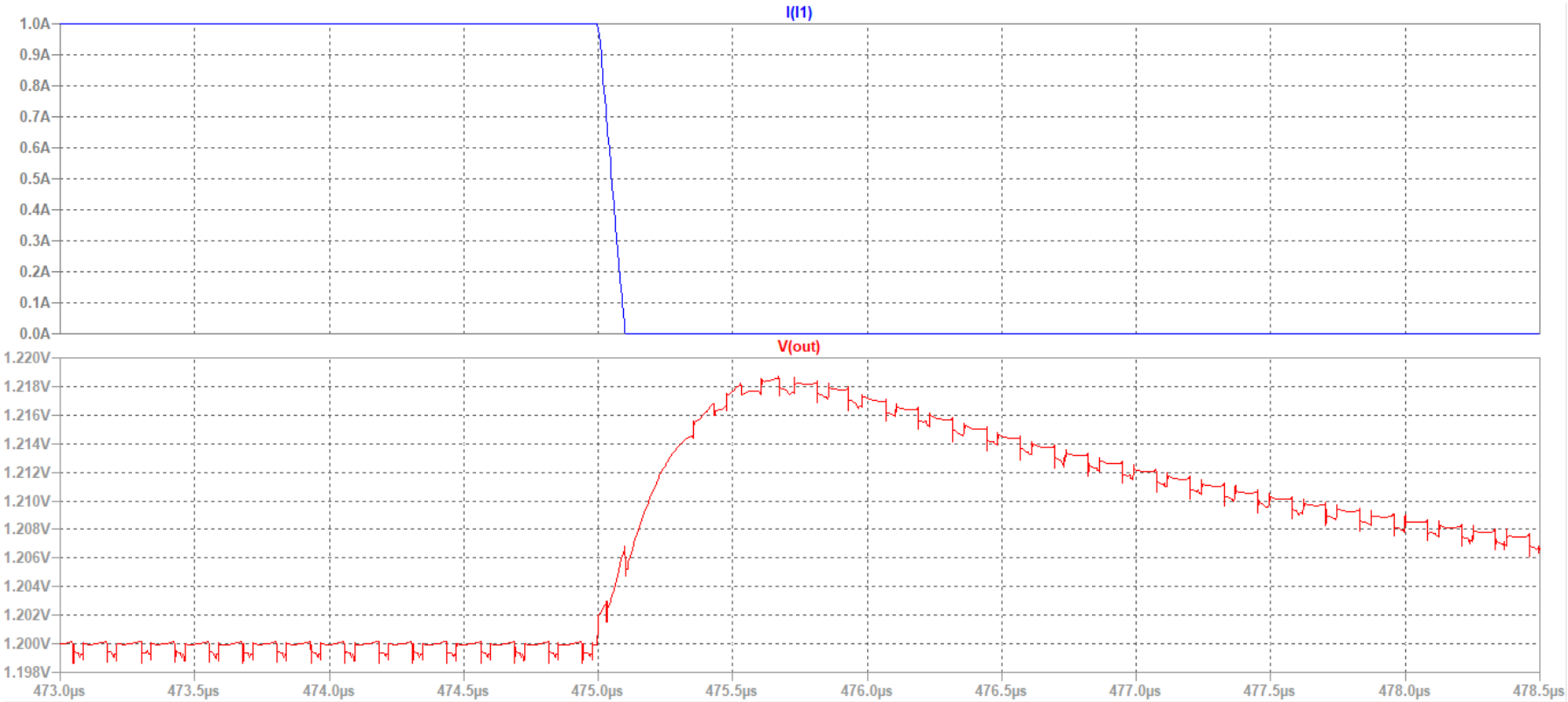


Figure: Load Transient Overshoot response for $V_{out} = 1.2V$

Simulation Results IV

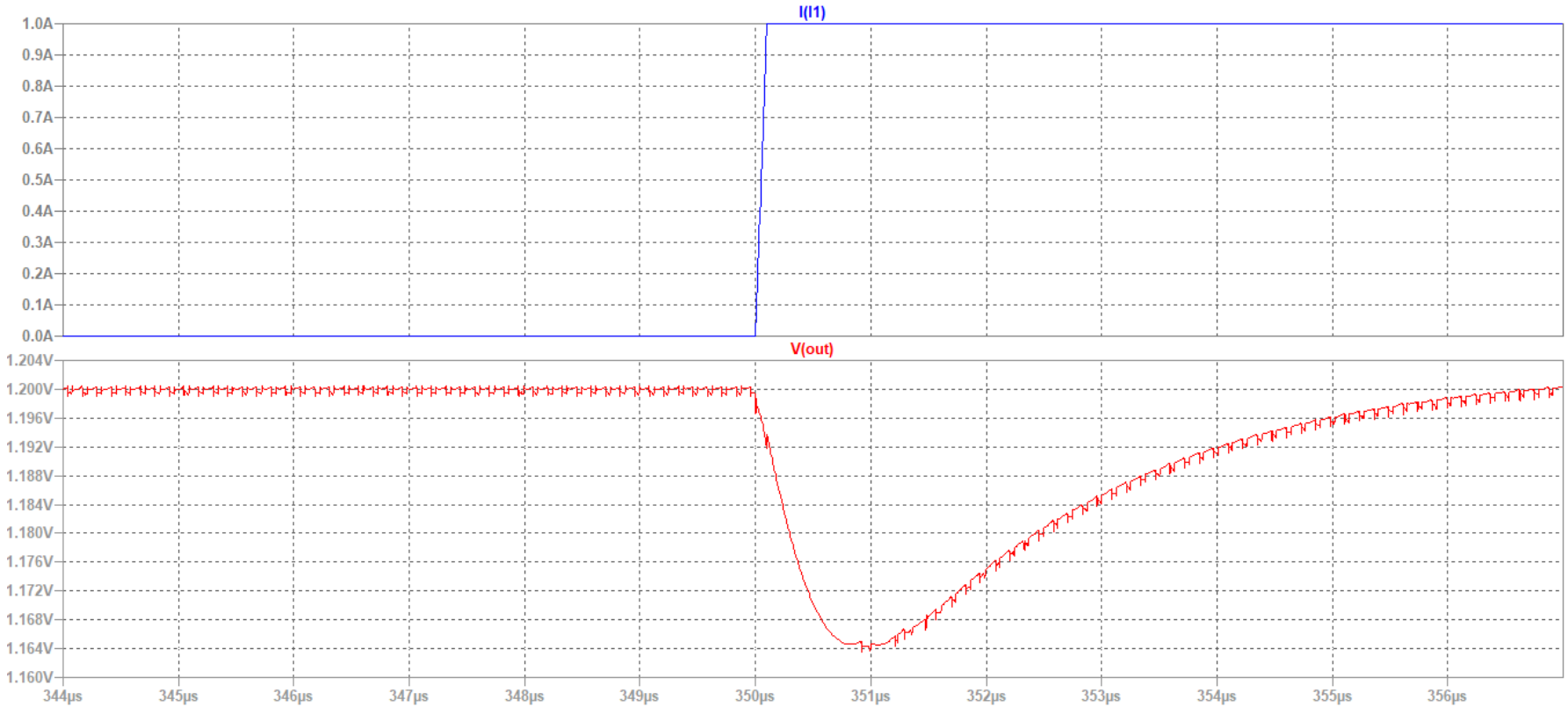


Figure: Load Transient Undershoot response for $V_{out} = 1.2V$

Simulation Results V

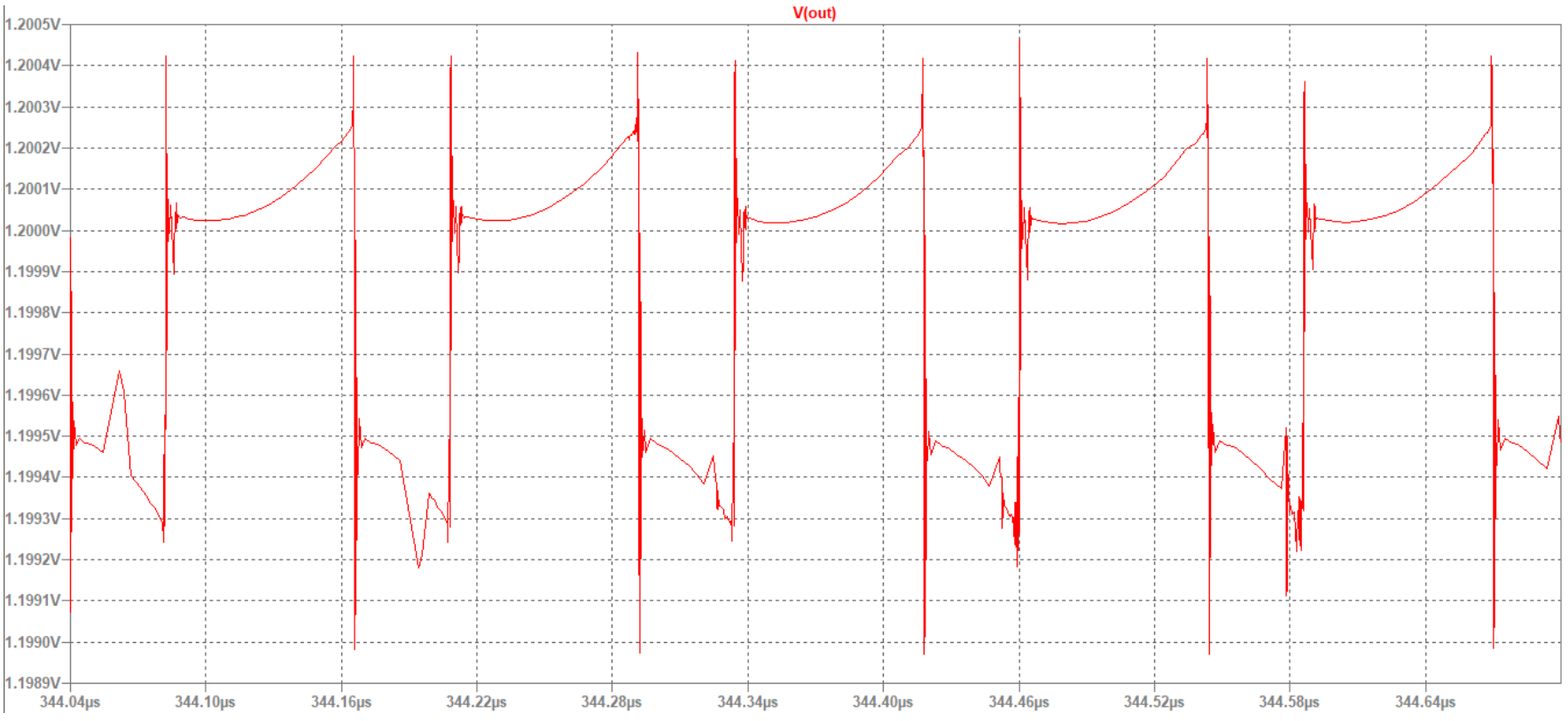


Figure: Output ripple for $V_{out} = 1.2V$

Performance Table - $V_{out} = 1.2V$

Parameters	**Results/Values (1mA)**	**Results/Values (1A)**
Settling time (PWM Cycles)	15	
DC output voltage inaccuracy	0.025%	0.05%
Overshoot (Load Transient)	1.586%	
Undershoot (Load Transient)	2.986%	
Overshoot (Line Transient)	0.589%	0.899%
Undershoot (Line Transient)	0.490%	0.547%
Efficiency (%)	11.76%	92.55%
Output ripple voltage (PWM)	916uVpp	1.53mVpp
FOM2	2.187×10^{-5}	

Table: Performance parameters for $V_{out} = 1.2V$

Short Circuit Protection - Simulation

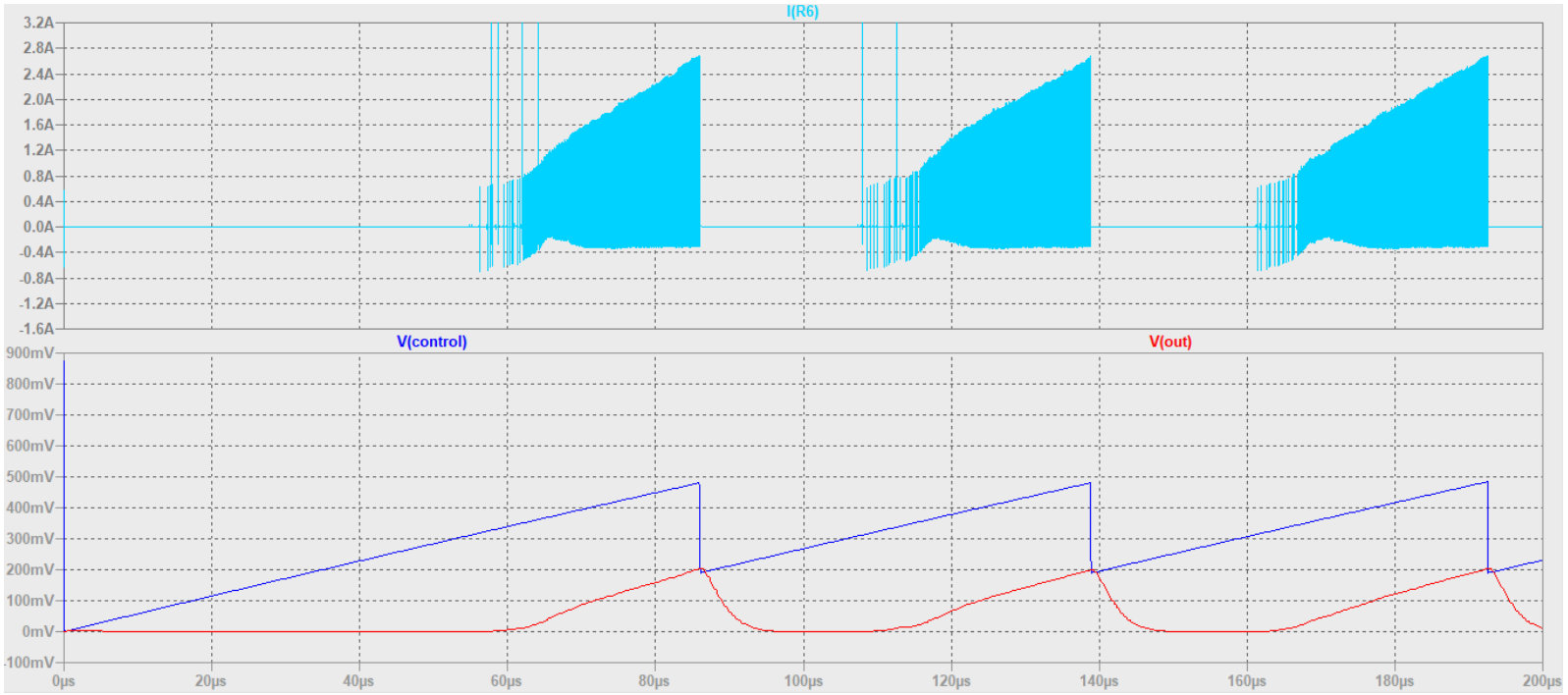


Figure: Transient response with Auto-Start up (Hicup mode)

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[2] Brian S Cherkauer and Eby G Friedman. "A unified design methodology for CMOS tapered buffers". In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 1 (1995), pp. 99–111.

[3] H Pooya Forghani-Zadeh and Gabriel A Rincón-Mora. "Low-power CMOS ramp generator circuit for DC-DC converters". In: *journal of low power electronics* 2.3 (2006), pp. 437–441.

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[6] Robert A. Mammano. *Applying the UCC3570 Voltage-Mode PWM Controller to both off-line and DC/DC Converter Designs*. Application Note. Texas Instruments, 1999.

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[10] Linear Technology, ed. *LT3479 - 3A, Full Featured DC/DC Converter with Soft-Start and Inrush Current Protection*.

[11] Michael Stokowski Tim Regan Jon Munson Greg Zimmer. *Current Sense Circuit Collection*. Application Note. Linear Technology Inc.